**FDS8817NZ**

**N-Channel PowerTrench® MOSFET**

30V, 15A, 7.0mΩ

**Features**

- Max $r_{DS(on)} = 7\text{mΩ}$ at $V_{GS} = 10\text{V}, I_D = 15\text{A}$
- Max $r_{DS(on)} = 10\text{mΩ}$ at $V_{GS} = 4.5\text{V}, I_D = 12.6\text{A}$
- HBM ESD protection level of 3.8kV typical (note 3)
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability
- RoHS compliant

**General Description**

This N-Channel MOSFET is produced using Fairchild Semiconductor’s advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance.

This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

### MOSFET Maximum Ratings

$T_A = 25\text{°C}$ unless otherwise noted

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Ratings</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>Drain to Source Voltage</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>Gate to Source Voltage</td>
<td>±20</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Drain Current</td>
<td>(Note 1a) 15</td>
<td>A</td>
</tr>
<tr>
<td>$E_{AS}$</td>
<td>Single Pulse Avalanche Energy</td>
<td>(Note 4) 181</td>
<td>mJ</td>
</tr>
<tr>
<td>$P_D$</td>
<td>Power Dissipation</td>
<td>(Note 1a) 2.5</td>
<td>W</td>
</tr>
<tr>
<td>$T_J, T_{STG}$</td>
<td>Operating and Storage Junction Temperature Range</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

**Thermal Characteristics**

- $R_{JUC}$ Thermal Resistance, Junction to Case (Note 1) 25 °C/W
- $R_{JUA}$ Thermal Resistance, Junction to Ambient (Note 1a) 50 °C/W
- $R_{JUA}$ Thermal Resistance, Junction to Ambient (Note 1b) 125 °C/W

**Package Marking and Ordering Information**

<table>
<thead>
<tr>
<th>Device Marking</th>
<th>Device</th>
<th>Reel Size</th>
<th>Tape Width</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDS8817NZ</td>
<td>FDS8817NZ</td>
<td>13&quot;</td>
<td>12mm</td>
<td>2500 units</td>
</tr>
</tbody>
</table>
## Electrical Characteristics \( T_J = 25°C \) unless otherwise noted

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \text{BV}_{\text{DSS}} )</td>
<td>Drain to Source Breakdown Voltage</td>
<td>( I_D = 250\mu A, \ V_{\text{GS}} = 0V )</td>
<td>30</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( \Delta \text{BV}_{\text{DSS}} )</td>
<td>Breakdown Voltage Temperature Coefficient</td>
<td>( I_D = 250\mu A, \text{ referenced to} 25°C )</td>
<td>20</td>
<td>mV/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{\text{DSS}} )</td>
<td>Zero Gate Voltage Drain Current</td>
<td>( V_{\text{DS}} = 24V, \ V_{\text{GS}} = 0V )</td>
<td>1</td>
<td>( \mu A )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{\text{GSS}} )</td>
<td>Gate to Source Leakage Current</td>
<td>( V_{\text{GS}} = 520V, \ V_{\text{DS}} = 0V )</td>
<td>±10</td>
<td>( \mu A )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Off Characteristics

### On Characteristics (Note 2)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{GS(th)}} )</td>
<td>Gate to Source Threshold Voltage</td>
<td>( V_{\text{GS}} = V_{\text{DS}}, \ I_D = 250\mu A )</td>
<td>1.8</td>
<td>3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( \Delta V_{\text{GS(th)}} )</td>
<td>Gate to Source Threshold Voltage Temperature Coefficient</td>
<td>( I_D = 250\mu A, \text{ referenced to} 25°C )</td>
<td>–6</td>
<td>mV/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( r_{\text{DS(on)}} )</td>
<td>Static Drain to Source On Resistance</td>
<td>( V_{\text{GS}} = 10V, \ I_D = 15A )</td>
<td>5.4</td>
<td>7</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>( r_{\text{DS(on)}} )</td>
<td>Static Drain to Source On Resistance</td>
<td>( V_{\text{GS}} = 4.5V, \ I_D = 12.6A )</td>
<td>7.0</td>
<td>10</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>( r_{\text{DS(on)}} )</td>
<td>Static Drain to Source On Resistance</td>
<td>( V_{\text{GS}} = 10V, \ I_D = 15A, \ T_J = 125°C )</td>
<td>7.5</td>
<td>11</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>( g_{\text{FS}} )</td>
<td>Forward Transconductance</td>
<td>( V_{\text{DS}} = 5V, \ I_D = 15A )</td>
<td>54</td>
<td>S</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Dynamic Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_{\text{iss}} )</td>
<td>Input Capacitance</td>
<td>( V_{\text{DS}} = 15V, \ V_{\text{GS}} = 0V, \ f = 1MHz )</td>
<td>1805</td>
<td>2400</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>( C_{\text{oss}} )</td>
<td>Output Capacitance</td>
<td>( V_{\text{DS}} = 15V, \ V_{\text{GS}} = 0V, \ f = 1MHz )</td>
<td>335</td>
<td>445</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>( C_{\text{rss}} )</td>
<td>Reverse Transfer Capacitance</td>
<td>( V_{\text{DS}} = 15V, \ V_{\text{GS}} = 0V, \ f = 1MHz )</td>
<td>200</td>
<td>300</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>( R_{\text{g}} )</td>
<td>Gate Resistance</td>
<td>( f = 1MHz )</td>
<td>1.4</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
</tbody>
</table>

### Switching Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{\text{d(on)}} )</td>
<td>Turn-On Delay Time</td>
<td>( V_{\text{DD}} = 15V, \ I_D = 15A )</td>
<td>11</td>
<td>22</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{r}} )</td>
<td>Rise Time</td>
<td>( V_{\text{GS}} = 10V, \ R_{\text{GEN}} = 6\Omega )</td>
<td>13</td>
<td>26</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{d(off)}} )</td>
<td>Turn-Off Delay Time</td>
<td>( V_{\text{DD}} = 15V, \ I_D = 15A )</td>
<td>25</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{f}} )</td>
<td>Fall Time</td>
<td>( V_{\text{GS}} = 0V ) to ( 10V )</td>
<td>7</td>
<td>14</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( Q_{\text{g}} )</td>
<td>Total Gate Charge</td>
<td>( V_{\text{GS}} = 0V ) to ( 10V )</td>
<td>32</td>
<td>45</td>
<td>nC</td>
<td></td>
</tr>
<tr>
<td>( Q_{\text{gs}} )</td>
<td>Gate to Source Charge</td>
<td>( V_{\text{DS}} = 0V ) to ( 5V )</td>
<td>17</td>
<td>24</td>
<td>nC</td>
<td></td>
</tr>
<tr>
<td>( Q_{\text{gd}} )</td>
<td>Gate to Drain “Miller” Charge</td>
<td>( V_{\text{DS}} = 5V, \ I_D = 15A )</td>
<td>6</td>
<td>nC</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Drain-Source Diode Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{SD}} )</td>
<td>Source to Drain Diode Forward Voltage</td>
<td>( V_{\text{GS}} = 0V, \ I_S = 2.1A ) (Note 2)</td>
<td>0.8</td>
<td>1.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{rr}} )</td>
<td>Reverse Recovery Time</td>
<td>( I_F = 15A, \ di/dt = 100A/\mu s )</td>
<td>24</td>
<td>36</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( Q_{\text{rr}} )</td>
<td>Reverse Recovery Charge</td>
<td>( I_F = 15A )</td>
<td>15</td>
<td>23</td>
<td>nC</td>
<td></td>
</tr>
</tbody>
</table>

#### Notes:

1. \( R_{\text{UA}} \) is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. \( R_{\text{JA}} \) is guaranteed by design while \( R_{\text{UA}} \) is determined by the user’s board design.

2. Pulse Test: Pulse Width < 300 us, Duty Cycle < 2%.

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

4. Starting \( T_J = 25°C, L = 3mH, I_A = 11A, V_{\text{DD}} = 30V, V_{\text{GS}} = 10V \).

---

![Image](a) 50°C/W when mounted on a 1in² pad of 2 oz copper.

b) 125°C/W when mounted on a minimum pad.
Typical Characteristics \( T_J = 25^\circ C \) unless otherwise noted

**Figure 1.** On-Region Characteristics

![On-Region Characteristics](image1)

**Figure 2.** Normalized On-Resistance vs Drain Current and Gate Voltage

![Normalized On-Resistance](image2)

**Figure 3.** Normalized On-Resistance vs Junction Temperature

![Normalized On-Resistance vs Junction Temperature](image3)

**Figure 4.** On-Resistance vs Gate to Source Voltage

![On-Resistance vs Gate to Source Voltage](image4)

**Figure 5.** Transfer Characteristics

![Transfer Characteristics](image5)

**Figure 6.** Source to Drain Diode Forward Voltage vs Source Current

![Source to Drain Diode Forward Voltage vs Source Current](image6)
**Typical Characteristics**  \( T_J = 25°C \) unless otherwise noted

**Figure 7.** Gate Charge Characteristics

**Figure 8.** Capacitance vs Drain to Source Voltage

**Figure 9.** Unclamped Inductive Switching Capability

**Figure 10.** Gate Leakage Current vs Gate to Source Voltage

**Figure 11.** Maximum Continuous Drain Current vs Ambient Temperature

**Figure 12.** Forward Bias Safe Operating Area
**Typical Characteristics**  \( T_J = 25^\circ C \) unless otherwise noted

![Figure 13. Single Pulse Maximum Power Dissipation](image)

![Figure 14. Transient Thermal Response Curve](image)

**FOR TEMPERATURES ABOVE 25°C DERATE PEAK CURRENT AS FOLLOWS:**

\[
I_p = I_{25} \left[ \frac{150 - T_A}{125} \right]
\]

\( T_A = 25^\circ C \)

**DUTY FACTOR:** \( D = \frac{t_1}{t_2} \)

\[
T_J = P_{DM} x Z_{θJA} x R_{θJA} + T_A
\]

**NOTES:**
TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE®
Across the board. Around the world.™
ActiveArray™
Bottomless™
Build it Now™
CoolFET™
CROSSVOLT™
CTL™
Current Transfer Logic™
E2CMOS™
EnSigna™
FACT Quiet Series™
FACT®
FAST®
FASTr™
FPS™
FRFET®
GlobalOptoisolator™
GTO™
HiSeCTM
i-LO™
ImpliedDisconnect™
IntelliMAX™
ISPLANAR™
MICROCOUPLER™
MicroPak™
MICROWIRE™
MSX™
MSXPro™
OCX™
OCXPro™
OPTOLOGIC®
OPTOPLANAR®
PACMAN™
POPTM
Power220®
Power247®
PowerEdge™
PowerSaver™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
RapidConnect™
ScalarPump™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™,3
SuperSOT™,6
SuperSOT™,9
SyncFET™
TCMTM
The Power Franchise®
TinyBoost™
TinyLogic®
TINYOPTO™
TinyPower™
TinyWire™
TruTranslation™
µSerDes™
UHC®
UniFET™
VCX™
Wire™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO
IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE
OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE
RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORL DWIDE TERMS AND CONDITIONS,
SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT
THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:
1. Life support devices or systems are devices or systems
which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when
properly used in accordance with instructions for use provided in
the labeling, can be reasonably expected to result in a significant
injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably
expected to cause the failure of the life support device or
system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

<table>
<thead>
<tr>
<th>Datasheet Identification</th>
<th>Product Status</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advance Information</td>
<td>Formative or In Design</td>
<td>This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.</td>
</tr>
<tr>
<td>Preliminary</td>
<td>First Production</td>
<td>This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.</td>
</tr>
<tr>
<td>No Identification Needed</td>
<td>Full Production</td>
<td>This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.</td>
</tr>
<tr>
<td>Obsolete</td>
<td>Not In Production</td>
<td>This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.</td>
</tr>
</tbody>
</table>