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REMOTE MONITORING OF EEG SIGNALS THROUGH WIRELESS SENSOR NETWORKS

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ABSTRACT

Electroencephalography, a measurement of the brain's electrical activity, has been used as a method of diagnosis and observation for patients with seizure disorders. However, it is often difficult to collect reliable and accurate data due to the relatively sensitive nature of most EEG hardware. Much of the artifacts and noise inherent in current EEG is a result of the movement of connecting wires. Toward that end, the intention of this project is to construct a two-channel EEG acquisition system and interface it with a Wireless Mesh Network. The system consists of a base station computer and a remote EEG collection system which can communicate via this mesh network. It is framed as a proof-of-concept model directed toward the eventual development of an entirely wire-free EEG system wherein each electrode is a miniature self-contained microprocessor node in a wireless mesh network.

The analog EEG portion was designed, built and found to pass all of the required tests. Likewise, the digital board and software were verified as functionally sufficient. The system was integrated successfully and tested for correct functionality.

BACKGROUND

EEG systems currently used in medical institutions are restricted in their application due to several physical limitations. One such limitation involves the signal artifacts created by movement of wires; even small movements of wires within the generated magnetic field causes artifacts of

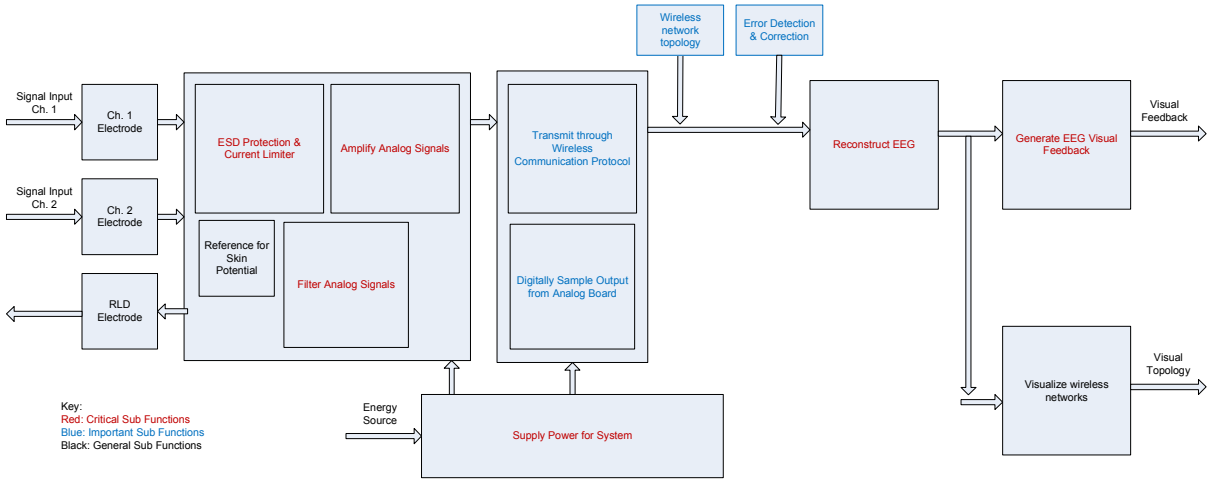

Figure 1: System Level Block Diagram of the Wireless EEG System

considerable magnitude. As these artifacts obstruct any analysis of procured EEG waveforms, the prevention of these artifacts would significantly improve the ability of medical professionals to perform accurate studies.

Consequently, a system in which each electrode functions as a data collection and conditioning node in a wireless mesh network offers a potential solution. A proof-of-concept system is proposed and implemented with the expectation that future iterations would be miniaturized. Ideally, each electrode will be small enough to be subdurally implanted in order to improve signal quality. Furthermore, implantation facilitates long term studies as it is less obtrusive than an external device.

Medical-grade EEG devices are quite expensive and carefully designed according to rigorous safety regulations and standards. Framing this project as a medical device design is infeasible given the allotted resources and time. For this reason, EEG hardware is designed based on an open source EEG project called OpenEEG. The OpenEEG schematics are proven as functionally sufficient, and they are freely available for non-commercial development. The proof-of-concept nature of this project makes the OpenEEG an ideal starting point for the analog design.

Wireless sensor networks are a popular area of research and application development. They offer a convenient and low-cost method of data collection for real-time applications. The Telosb wireless hardware platform is chosen as the prototypical wireless node for this project due to the fact that it is open source and is designed for interfacing with a variety of sensors. It is also extremely low-power and convenient to program and develop making it ideal for this application.

TinyOS is utilized as the operating system on the nodes as it is a popular software platform for use with wireless networks. It is formulated as a low-power, low-footprint operating system that can be run on wireless devices with limited resources. It is also popular due to its robust libraries and active online community. These advantages make it an appropriate platform with which to develop and implement the design.

PROCESS

The wireless EEG project aims to develop a platform that enables devices to be wirelessly connected to each other as part of a mesh network. An analog EEG board is designed to acquire EEG signals from a human subject. The signals are appropriately processed (amplified and filtered) and wirelessly transmitted to a base station as digitized information packets. The design is split into two primary segments—the analog board design and the digital board design. A system level block diagram is shown in Figure 1.

A number of different design possibilities are explored for each stage and their advantages and disadvantages are weighed. Each option is researched for performance, reliability and feasibility of implementation. Figure 2 summarizes the possibilities considered for each stage and the final configuration chosen.

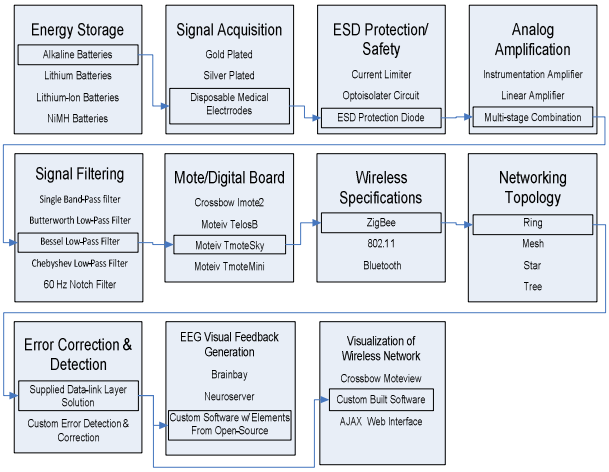

Figure 2: Design and System Choices for Individual Stages

The first major subsystem of the design is the analog circuit responsible for acquisition and conditioning of EEG data. The analog board is designed to amplify low voltage differential EEG signals in the frequency range of interest. It attenuates unwanted high and low frequency signals using appropriate filtering mechanisms. The key specifications for the analog board include:

- Single Supply Operation
- Low Power Consumption
- Portable and Lightweight Design
- Adjustable Gain
- High Signal Integrity

Table 1 summarizes the quantitative performance specifications of the analog board. Additionally, the results of the tests conducted on the board are also summarized in Table 1.

Specification Type	Acceptable Operational Values	Testing Status	
		PSPICE Simulations	Hardware
Input Battery Voltage	5.6V (± 0.4V)	Pass	Pass
Circuit Operating Voltage	5.0V (± 0.1V)	Pass	Pass
Analog Board Power Consumption	≤ 150mW (± 10mW)	Pass	Pass
Input EEG Signal Frequency Range of Interest	0.16Hz to 30Hz	Pass	Pass
EEG Input Signal Voltage	1μV to 1mV	Pass	Pass
Total Analog Board Voltage Gain Range	4500V/V ± 1000V/V	Pass	Conditional Pass
Common Mode Rejection Ratio	≥ 110dB ± 20dB	Pass	Pass
Amplifier Input Impedance	100MΩ	Pass	Pass
Low Pass Filter (3rd Order Active Bessel Filter) fC	60Hz ± 5Hz	Pass	Pass
High Pass Filter (2nd Order Passive RC Filter) fC	0.16Hz ± 0.25Hz	Pass	Pass
Weight	300 grams (≤ 500 grams)	Pass	Pass
Size	6 inches x 6 inches (max)	Pass	Pass
Operating Temperature	21°C ± 25°C	Pass	Pass

Table 1: Summary of Analog Board Quantitative Specifications and Testing Status.

A fundamental block diagram of the analog board is shown in Figure 3.

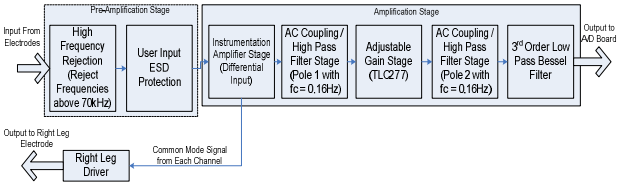

Figure 3: System Level Block Diagram for the Analog Board

The analog board design is primarily based on the OpenEEG project. However, several modifications are made to the Open EEG circuit to enhance performance. An ESD protection diode is used to safeguard the circuit against an ESD discharge instead of a transistor network due to reliability issues. In the implementation of the virtual ground circuit, the buffered divider network topology is replaced by a voltage reference chip. A zener diode is also added at the end of the design to ensure that the output going to the A/D converter is clamped at a maximum of 2.4V. An adjustable gain stage is also added to the design to make the circuit modifiable to suit user needs. The circuit design is first implemented in PSPICE to verify performance. The design is split into several smaller stages and each one is individually tested and analyzed. Figure 4 through Figure 9 show the individual stages of the design and the corresponding simulation results.

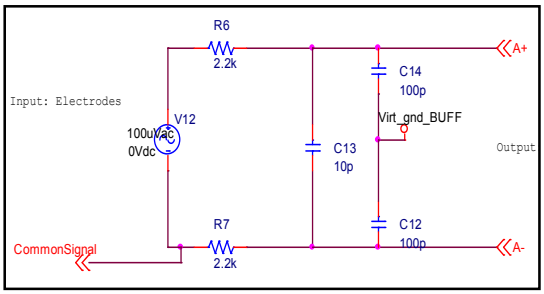

Figure 4: High Frequency Rejection Circuit with its output going to the Instrumentation Amplifier Stage through an ESD Protection Diode

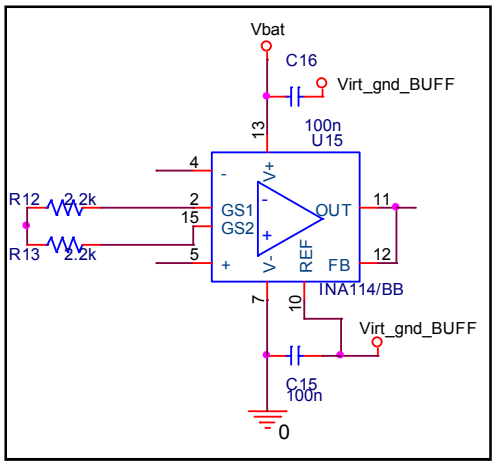

Figure 5: Instrumentation Amplifier Stage implemented using the INA114 amplifier

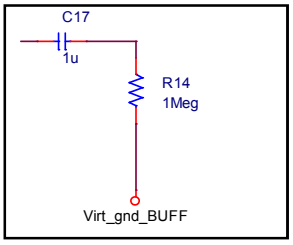

Figure 6: One of two Passive High Pass Filters used to define the lower cutoff frequency of the amplifier

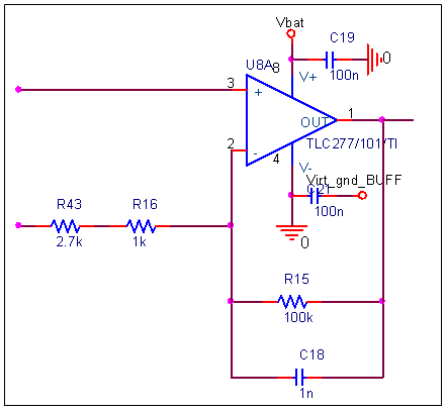

Figure 7: Adjustable Gain Stage implemented using the TLC277 operation amplifier

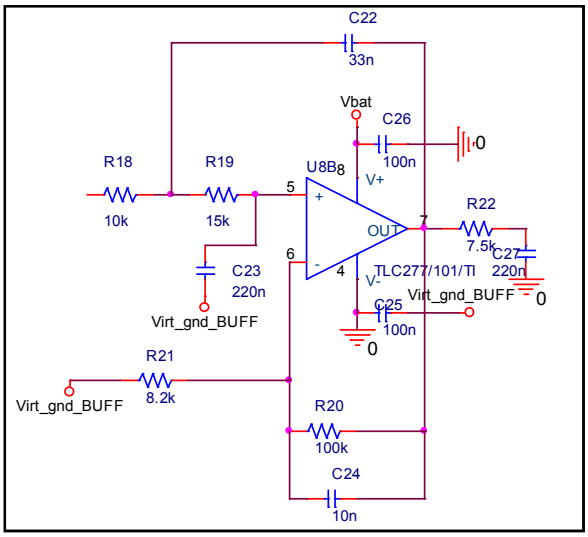

Figure 8: 3rd Order Low Pass Bessel Filter Stage implemented using the TLC 277 operational amplifier

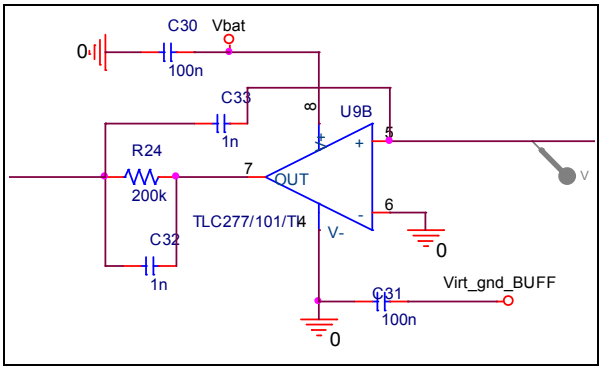

Figure 9: Right Leg Drive Circuit

The performance of the board is rigorously tested through a variety of tests. The prominent tests conducted to verify key performance specifications are summarized towards the end of this section. Table 1 summarizes the results of the test plan.

For the hardware aspect of the project, the board is laid out using EaglePCB. A two layer board with SMT components is designed and manufactured through BatchPCB.com. The trace diagram of the board is shown in Figure 10. The facilities at RIT's Center for Electronics Manufacturing and Assembly Lab are used to solder the components on the board.

The second principle subsystem entails the wireless transmission of digitized EEG data to a base station for analysis. This system has three key components; the remote hardware to digitize and transmit data, the base station computer, and software to achieve the desired functionality on the aforementioned hardware.

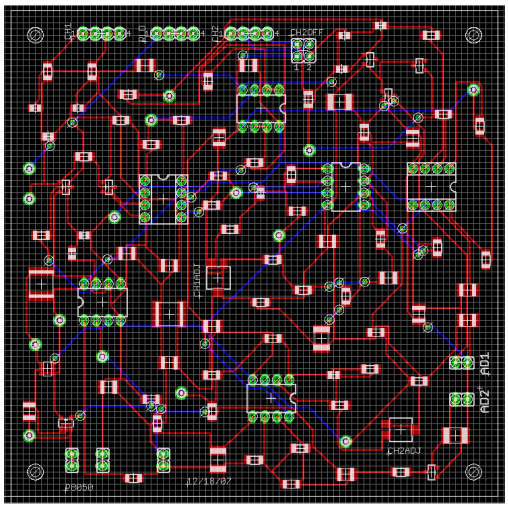

Figure 10: Trace Diagram for the Analog Board Design

Specification	Units	Value	Tolerances
Power Consumption	mW	69	5
Wireless Transmission Reliability	% packet loss	0.1	N/A
Resolution of ADC	bits	12	N/A
Dynamic Range of ADC	dB	60	N/A
Sampling Rate	Hz	250	N/A
Bandwidth Per User	bits/s	7,920	N/A
Maximum Number of Users Per System	Devices	3	N/A
Size of Software Image	KBytes	48	N/A

Table 2: Summary of Digital Board Quantitative Specifications

Rather than design a system to sample, packetize, and transmit EEG data, a device encompassing all these functions and designed specifically for remote sensing is selected as the optimal solution with the given resources. These devices, called "motes", feature power-efficient microprocessors and transmitters and, most importantly, support a variety of platforms designed to facilitate software development for wireless sensing applications. Requirements of such a device include: available bandwidth, minimal power consumption, physical size, memory provided, and at least two ADC channels with sufficient sampling frequency and resolution. The open-source TelosB mote, manufactured by Crossbow, is chosen as the device which best fulfills these needs. The TelosB mote features a TI MSP430F1611 microprocessor in conjunction with a Chipcon CC2420 2.4 GHz ZigBee transceiver. Furthermore, the TelosB mote is well supported by the TinyOS operating environment; the TinyOS platform is an event driven operating system which facilitates low-power software development on motes.

Additionally, TinyOS provides a framework for simple development of a wireless infrastructure. This framework is configured and customized in order to meet the requirements of the desired system; namely, each analog circuit/mote pair acts as a node in a wireless mesh network, and transmits digitized EEG data to the base station. The base station receives data via a connected "gateway" mote, which transmits packets through a USB connection. Software on the base station is developed for the purpose of interfacing with the gateway mote, parsing received packets, plotting data, and configuring devices. This is made possible by a Java API provided in the TinyOS framework. The software features a GUI which facilitates control/configuration of devices and analysis of received data.

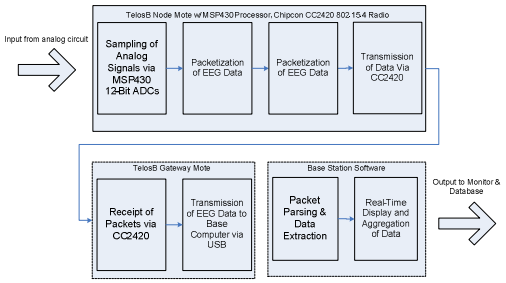

Figure 11: Digital/Software Flow Chart

The embedded device software makes use of platform specific TinyOS libraries in order to simplify interfacing with individual hardware components. The software collects data from two multiplexed ADC channels on the mote at a constant interval of 4ms, buffers it in order to ensure data integrity, encapsulates the data within a packet, and transmits it to the gateway mote. In the meantime, messages are constantly disseminated from each device in order to calculate the link cost to any neighbors and update the routing table accordingly; this is performed in order to ensure a high-performance, self-healing mesh network. The TinyOS event-driven application model allows for components to enter a low-power "sleep" mode while not in use. Concurrent processing necessitates careful attention to resource management and prioritization of competing threads.

The base station software communicates with the gateway mote via a TinyOS java library; this library simplifies access to the mote through the USB RS232. The software then parses the transmitted packets, converting the ADC counts into voltage readings, and plotting them with the LiveGraph Java library.

The two subsystems are independently tested and then tested as a single unit. The primary tests that verify key performance specifications are as follows.

Square-Wave Calibration Test

A function generator is set-up to apply a square wave of 100 μV_{p-p} amplitude at a frequency of 1 Hz to the input of the EEG amplifier. To obtain a signal amplitude of 100μV_{p-p}, a voltage divider is used. This signal is used to drive each channel independently while grounding the unused inputs. An oscilloscope is used to verify that the output has a required gain of 4500 V/V ± 400V/V.

Anti-Aliasing High-Filter Test

Prior to sampling at 256 samples/second, an anti-aliasing high filter at 70 Hz must be used, with a roll-off of at least 12 dB/octave. The function generator is setup to output a sine wave with a $1mV_{pp}$ amplitude at a frequency of 1.0 kHz. According to the simulated results, the gain at 1kHz should be about 0dB. The sine wave signal is applied to the electrodes of one channel. The right leg driver is connected to ground and the unused channel inputs are also grounded. Using an oscilloscope, the gain is measured at the output. A gain of 0dB is expected. This procedure is repeated for the second channel.

Low Filter Test

Retaining the set-up from the High Filter Test, the gain of the amplifier is measured at about 2mHz. Using an oscilloscope, the gain is measured at the output. A gain of 0dB is expected at 2mHz. This procedure is repeated for the second channel.

Common Mode Rejection Ratio (CMRR) Test

The common mode rejection ratio of the amplifier must be at least 110 dB for each channel. A 0.1mV differential signal at and a $3V_{p-p}$ common signal are applied to one channel of the amplifier (both at 10Hz) while the other channel and the right leg driver are both grounded. Using an oscilloscope, the gains of each mode are measured and the CMRR is calculated using equation (1). This procedure is repeated for the second channel.

$$CMRR = 20\log\left(\frac{GAIN_{Differential\ Mode}}{GAIN_{Common\ Mode}}\right) \qquad (1)$$

Power Consumption

The power consumption must be 150mW +/- 10mW for the analog part of the design and 69mW +/- 5mW for the digital portion. A DC Power Supply is setup to output 6V for the analog board while an input signal of $.1mV_{pp}$ is applied at 10Hz. The power to the board is routed through an ammeter to measure the current drawn. The applied voltage is measured using a voltmeter and the current shown on the ammeter is recorded. The power consumption is calculated using (2). The procedure is repeated for the digital board with the exception that a supply voltage of 3VDC is applied.

$$Power = Voltage\ Applied \times Current\ Drawn \qquad (2)$$

Simulated EEG Waveform Test

An EEG waveform is modeled in MATLAB and applied to the EEG amplifier using an arbitrary function generator. The output on the oscilloscope is observed to ensure that the appropriate gain and filtering are being applied.

Digital Frequency and Amplitude Verification

The waveform generator is set to output a signal with $1V_{pp}$ amplitude at a frequency of 20 Hz. The signal is applied to channel one after grounding the second channel and the right leg driver. The output of the analog portion is connected to ADC0 of the microprocessor. Digital samples of the signal are acquired and samples are plotted in MATLAB to verify the amplitude. The FFT of the samples is also plotted to verify the appropriate frequency content.

Scalability Test

Two motes are simultaneously connected and the Amplitude Range and Digital Frequency tests are performed to verify system scalability.

Multihop Verification

A connection is established to a device using the software and sampling is initiated. A second device is placed beyond the range of the intermediary device and sampling is also initiated with it. The removal of the intermediary device will break the multi-hop (mesh) connection to the base station. The intermediary device is added back into the network and reconnection of the out-of-range device is observed.

RESULTS AND DISCUSSION

The manufactured and populated analog board is shown in Figure 12.

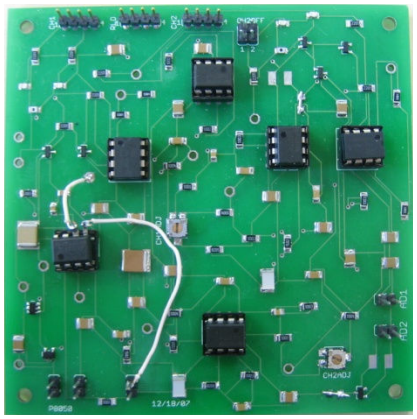

Figure 12: Completed Analog EEG Board

Several tests are conducted to ensure that the analog board performance meets specifications. Table 1shows the status of all the tests conducted on the board. The gain of the amplifier is reduced to 2000V/V ± 200V/V because the virtual ground voltage is readjusted to 1.25V during implementation. With the readjusted virtual ground voltage, a gain of 4500V/V would have caused the output to clip, so the change in specifications is implemented. The gain of the board can, however, be easily adjusted using the potentiometer in the adjustable gain stage. A gain of 2000V/V is successfully achieved when, as shown in Figure 13, an input signal of 100µV (at 10 Hz) is applied and an output of 200mV is obtained. Since, the specifications are modified for this test it is given a *Conditional Pass* status.

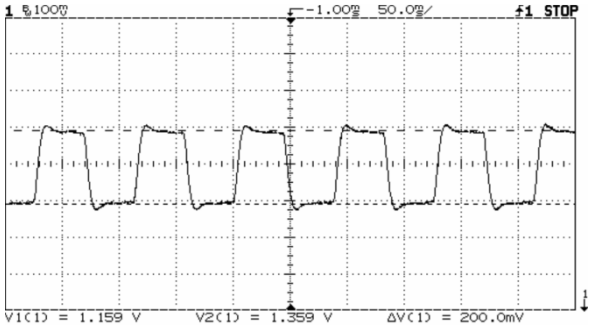

Figure 13: Square Wave Calibration Test Output

In the implementation of the high filter test, a $3mV_{pp}$ signal is applied, but at 1kHz the output is $12.5mV_{pp}$ instead of $3mV_{pp}$. Unity gain is attained at a frequency of 1.8kHz. However, more importantly, the cutoff frequency of the high filter is at 62Hz which is within the specified limits. The cutoff frequency of the low filter is experimentally determined to be about 300mHz which is also within the specified limits.

It is essential that the gain of the amplifier be constant throughout the pass band of the amplifier. The differential gain of the amplifier is experimentally measured for a range of frequencies and is plotted as shown in Figure 14. As seen in the plot, the gain is constant throughout the pass band as desired. Moreover, the pass band extends from 300mHz to 62Hz which is within the specified limits.

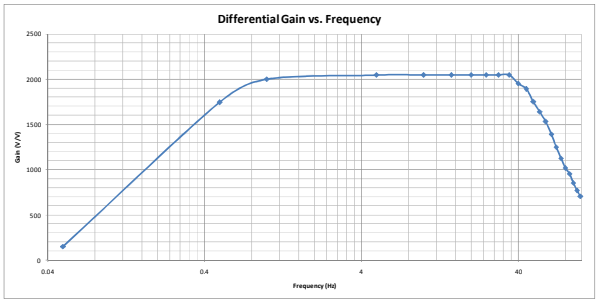

Figure 14: Differential Gain Vs. Frequency Plot for the EEG Amplifier

CMRR reflects the amplifier's ability to reject noise common to both inputs and is a key performance feature. The CMRR is calculated using (1) for a range of different frequencies and plotted in Figure 15 as shown. As required by the specifications, the CMRR of the amplifier is greater than 110dB in the pass band of the amplifier.

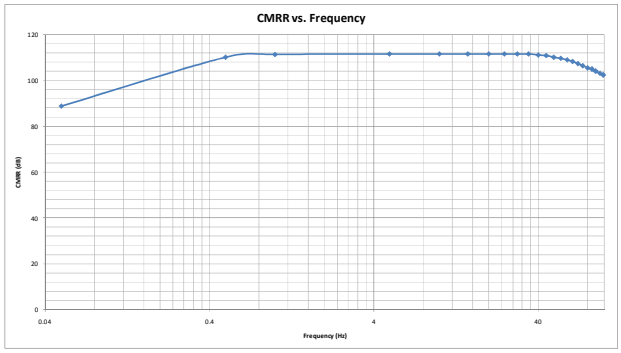

Figure 15: CMRR Vs Frequency for the EEG Amplifier

Since the device is battery operated, the power consumption of the board is also closely monitored. As shown in Table 1, the maximum power consumption is observed when the input signal is highest. For a $1mV_{pp}$ input, the current drawn is 8.21mA and the applied voltage is 6.327V. Thus, the worst case power consumption of the analog board is 51.88mW, which is well within the required limits. The power consumption measurements for different input signal amplitudes are summarized in Table 3.

Input Signal Amplitude (uV)	Voltage Applied (V)	Current Drawn (mA)	Power (mW)
1	6.327	5.504	34.82
10	6.327	5.507	34.84
100	6.327	5.515	34.89
500	6.327	5.960	37.71
1000	6.327	8.210	51.94

Table 3: Summary of Analog Board Power consumption

The power consumption of the digital board is also experimentally measured. The maximum current drawn by the digital board is measured to be 25.87mA when the applied voltage is 3.2V. Thus, the worst case power consumption of digital board is about 83mW. Adding the power consumed by the individual subsystems, it can be concluded that the power consumed by the system as a whole is less than the 150mW specification.

Real EEG data is also plotted using MATLAB and applied as an input to the amplifier using an arbitrary function generator. The input to the amplifier and the processed output are shown in Figure . The expected gain is achieved for the signal and no frequency content appears to be lost. The functionality of the analog board is thus verified and all the tests yield satisfactory results.

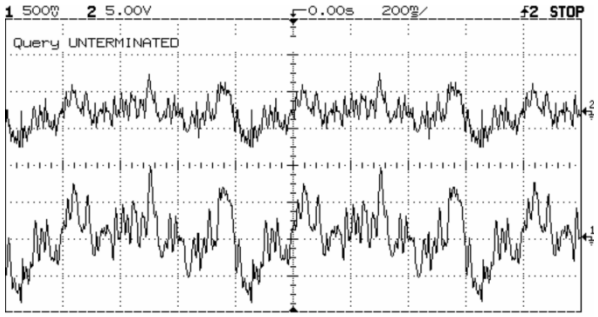

Figure 15: Sample EEG input signal (Top) and the processed output signal (Bottom) from the amplifier. Note that the input signal is divided by a factor of 10000 using a voltage divider before being applied to the amplifier.

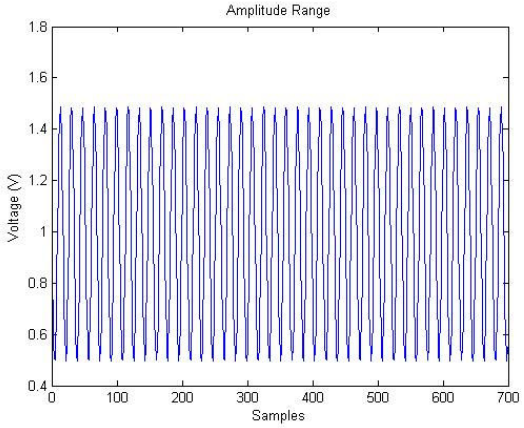

Figure 16: Amplitude Range of Sampled Test Signal

The digital board is tested according to the tests described above. First, the sampling and transmission is tested according to the Amplitude Range test. The results of this are shown in Figure 15. The accuracy of the signal is clearly visible. Figure 16 shows the Fast Fourier Transform of the same test signal. It is thus clear that the correct frequency signal was obtained by the digital board and software.

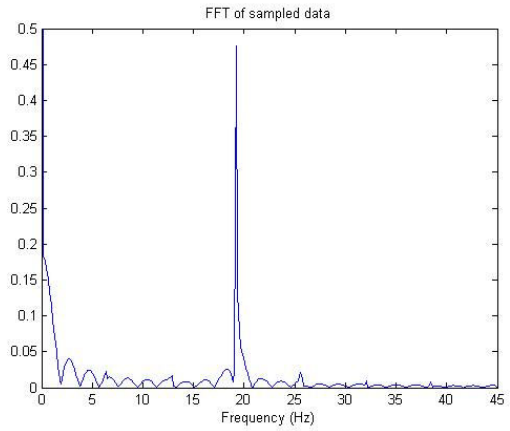

Figure 17: FFT of Sampled Test Signal

The scalability test is performed to determine whether the system can be extended to use multiple nodes. Connections are established to more than one mote and the transmission of packets is verified. The test was successfully run by the wireless system.

The multihop verification Test is performed on three motes. Since there was only one assembled analog board, the other mote transmitted samples of an open pin. The wireless network multihop functionality was found to be adequate.

CONCLUSIONS AND RECOMMENDATIONS

Based on the test results, it can be concluded that the analog board design meets all the requirements of an EEG acquisition and processing system. All the design specifications of the board are successfully verified through tests. Key performance features like gain, frequency response, and CMRR adhere to the design requirements. Moreover, all power consumption requirements are met. The system is tested with simulated and real EEG signals, and all results indicate a successful implementation of the design.

In spite of some integration difficulties the digital board is capable of sampling a signal within the appropriate EEG frequency range and transmitting it to the base station. During the initial development of the sampling and transmission system, the reconstructed test signal appeared to be accurate, but upon integration it is shown that there are unforeseen accuracy issues with the ADC and embedded software while sampling real signals. This issue indicates an area that could be improved in future projects.

The software subsystem of this project features a robust design with a significant set of features for the end user. It is highly modular, and it can be applied in almost any remote data collection scenario. The ability to separate the specific hardware and data type from the system as a whole adds an element of reusability if this proves reasonable for alternative projects.

Based on the issues that arose during the implementation of the design, a number of improvements can be suggested for future iterations of this system. In its current form, the analog board and the digital board operate on different supply voltages. The digital board is powered using 4 AA batteries while the digital board uses only two. As a result, two of the four batteries are consumed at a greater rate. Ideally, the entire system should be powered using the same supply voltage.

Another limitation of the analog board design is its size. The board is laid out on a 4”x4” footprint which can be considerably reduced in future iterations. The use of active electrodes in future implementations will also be a significant design improvement.

In the digital portion of the system, it was found that the Telosb platform is limited in its ability to buffer and store data before sending it onto its network. The use of a platform with more internal resources for data management would greatly streamline the process of collecting and transmitting large amounts of data.

Some of the hardware present on the Telosb platform is also sub-optimal for sensitive data collection applications. Improvements to the ADC and the power management of the processor would have a beneficial impact on the entire system’s performance.

ACKNOWLEDGMENTS

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