NanoPower Supervisory Circuits

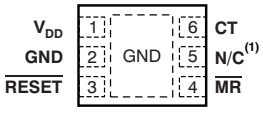
FEATURES

- **Supply Current: 220 nA (typical)**
- **Precision Supply Voltage Supervision Range: 1.8 V, 2.5 V, 3.0 V, and 3.3 V**
- **Power-On Reset Generator With Selectable Delay Time: 10 ms or 200 ms**
- **Push/Pull $\overline{\text{RESET}}$ Output (TPS3836), $\overline{\text{RESET}}$ Output (TPS3837), or Open-Drain $\overline{\text{RESET}}$ Output (TPS3838)**
- **Manual Reset**
- **SOT23-5 and 2x2 SON-6 Packages**
- **Temperature Range: –40°C to +85°C**

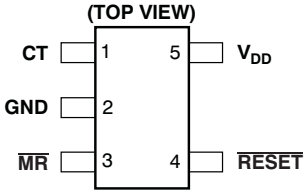
APPLICATIONS

- **Applications Using Low-Power DSPs, Microcontrollers, or Microprocessors**
- **Portable- and Battery-Powered Equipment**
- **Intelligent Instruments**
- **Wireless Communication Systems**
- **Notebook Computers**
- **Automotive Systems**
- **Applications Using the MSP430™**

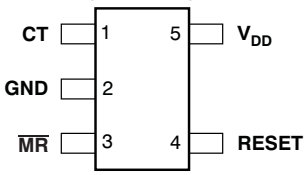
TPS3838DRV
2mm x 2mm SON-6
(TOP VIEW)



TPS3836, TPS3838
DBV PACKAGE
(TOP VIEW)



TPS3837
DBV PACKAGE
(TOP VIEW)



(1) N/C: Not connected.

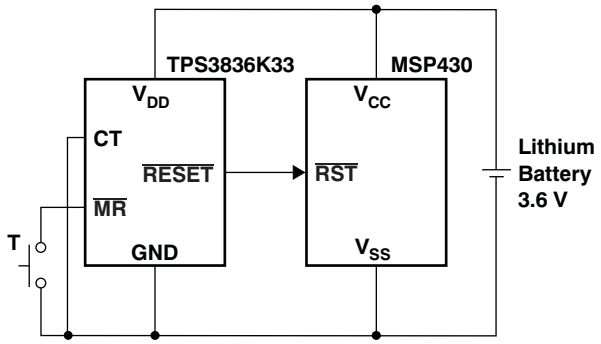
DESCRIPTION

The TPS3836, TPS3837, and TPS3838 families of supervisory circuits provide circuit initialization and timing supervision, primarily for DSP and processor-based systems.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps the $\overline{\text{RESET}}$ output active as long as V_{DD} remains below the threshold voltage of V_{IT}. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after V_{DD} has risen above the threshold voltage V_{IT}.

When CT is connected to GND, a fixed delay time of typical 10 ms is asserted. When connected to V_{DD}, the delay time is typically 200 ms. When the supply voltage drops below the threshold voltage V_{IT}, the output becomes active (low) again. All the devices of this family have a fixed-sense threshold voltage (V_{IT}) set by an internal voltage divider.

The TPS3836 has an active-low, push-pull $\overline{\text{RESET}}$ output. The TPS3837 has an active-high, push-pull RESET, and the TPS3838 integrates an active-low, open-drain $\overline{\text{RESET}}$ output. The product spectrum is designed for supply voltages of 1.8 V, 2.5 V, 3.0 V, and 3.3 V. The circuits are available in either a SOT23-5 or 2x2 SON-6 package. The TPS3836, TPS3837, and TPS3838 families are characterized for operation over a temperature range of –40°C to +85°C.



Typical Application Circuit

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	NOMINAL SUPPLY VOLTAGE	THRESHOLD VOLTAGE (V_{IT})(2)
TPS383xE18	1.8 V	1.71 V
TPS383xJ25	2.5 V	2.25 V
TPS383xH30	3.0 V	2.79 V
TPS383xL30	3.0 V	2.64 V
TPS383xK33	3.3 V	2.93 V

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Custom threshold voltages are available. Minimum order quantities apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	TPS383xx	UNIT
Supply voltage, V_{DD}(2)	7	V
All other pins(2)(3)	–0.3 to 7	V
Maximum low output current, I_{OL}	5	mA
Maximum high output current, I_{OH}	–5	mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	±10	mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	±10	mA
Continuous total power dissipation	See Dissipation Ratings Table	
Operating temperature range, T_A	–40 to +85	°C
Storage temperature range, T_{STG}	–65 to +150	°C
Soldering temperature	+260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) If RESET or $\overline{\text{RESET}}$ are pulled above V_{DD}, the internal ESD structure will present an effective 1.5 kΩ resistor between these pins, causing leakage current to flow into the RESET or $\overline{\text{RESET}}$ pin.

DISSIPATION RATINGS

PACKAGE	T_A < +25°C POWER RATING	DERATING FACTOR ABOVE T_A = +25°C	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
DBV	437 mW	3.5 mW/°C	280 mW	227 mW
DRV Low-K(1)	715 mW	7.1 mW/°C	395 mW	285 mW
DRV High-K(2)	1540 mW	15.4 mW/°C	845 mW	615 mW

(1) The JEDEC low-K (1s) board used to derive this data was a 3in x 3in, two-layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3in x 3in, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on the top and bottom of the board.

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1.6	6	V
Voltage range, CT, $\overline{MR}$, RESET, and $\overline{RESET}$ pins	0	V_{DD} + 0.3	V
High-level input voltage, V_{IH}	0.7 × V_{DD}		V
Low-level input voltage, V_{IL}		0.3 × V_{DD}	V
Input transition rise and fall rate at $\overline{MR}$, Δt/ΔV		100	ns/V
Operating temperature range, T_A	–40	+85	°C

ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{RESET}$ (TPS3836)	V_{DD} = 3.3 V, I_{OH} = –2 mA	0.8 × V_{DD}			V
			V_{DD} = 6 V, I_{OH} = –3 mA				
		RESET (TPS3837)	V_{DD} = 1.8 V, I_{OH} = –1 mA				
			V_{DD} = 3.3 V, I_{OL} = –2 mA				
V_{OL}	Low-level output voltage	$\overline{RESET}$ (TPS3836, TPS3838)	V_{DD} = 1.8 V, I_{OL} = 1 mA			0.4	V
			V_{DD} = 3.3 V, I_{OL} = 2 mA				
		RESET (TPS3837)	V_{DD} = 3.3 V, I_{OL} = 2 mA				
			V_{DD} = 6 V, I_{OL} = 3 mA				
	Power-up reset voltage(1)	TPS3836, TPS3838	V_{DD} ≥ 1.1 V, I_{OL} = 50 µA			0.2	V
		TPS3837	V_{DD} ≥ 1.1 V, I_{OL} = –50 µA	0.8 × V_{DD}			V
V_{IT}	Negative-going input threshold voltage(2)	TPS383xE18	T_A = –40°C to +85°C	1.66	1.71	1.74	V
		TPS383xJ25		2.18	2.25	2.29	
		TPS383xH30		2.70	2.79	2.85	
		TPS383xL30		2.56	2.64	2.69	
		TPS383xK33		2.84	2.93	2.99	
V_{HYS}	Hysteresis at V_{DD} input		1.7 V < V_{IT} < 2.5 V		30		mV
			2.5 V < V_{IT} < 3.5 V		40		
			3.5 V < V_{IT} < 5 V		50		
I_{IH}	High-level input current	$\overline{MR}$ (3)	$\overline{MR}$ = 0.7 × V_{DD}, V_{DD} = 6 V	–40	–60	–100	µA
		CT	CT = V_{DD} = 6 V	–25		+25	nA
I_{IL}	Low-level input current	$\overline{MR}$ (3)	$\overline{MR}$ = 0 V, V_{DD} = 6 V	–130	–200	–340	µA
		CT	CT = 0 V, V_{DD} = 6 V	–25		+25	nA
I_{OH}	High-level output current	TPS3838	V_{DD} = V_{IT} + 0.2 V, V_{OH} = V_{DD}			25	nA
I_{DD}	Supply current		V_{DD} > V_{IT}, V_{DD} < 3 V		220	400	nA
			V_{DD} > V_{IT}, V_{DD} > 3 V		250	450	
			V_{DD} < V_{IT}		10	15	µA
	Internal pull-up resistor at $\overline{MR}$				30		kΩ
C_I	Input capacitance at $\overline{MR}$ and CT		V_I = 0 V to V_{DD}		5		pF

(1) The lowest voltage at which the $\overline{RESET}$ output becomes active. t_R, V_{DD} ≥ 15 µs/V.
(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near the supply terminal.
(3) If manual reset is unused, $\overline{MR}$ should be connected to V_{DD} to minimize current consumption.

SWITCHING CHARACTERISTICS

At T_A = +25°C, R_L = 1 MΩ, and C_L = 50 pF, unless otherwise noted.

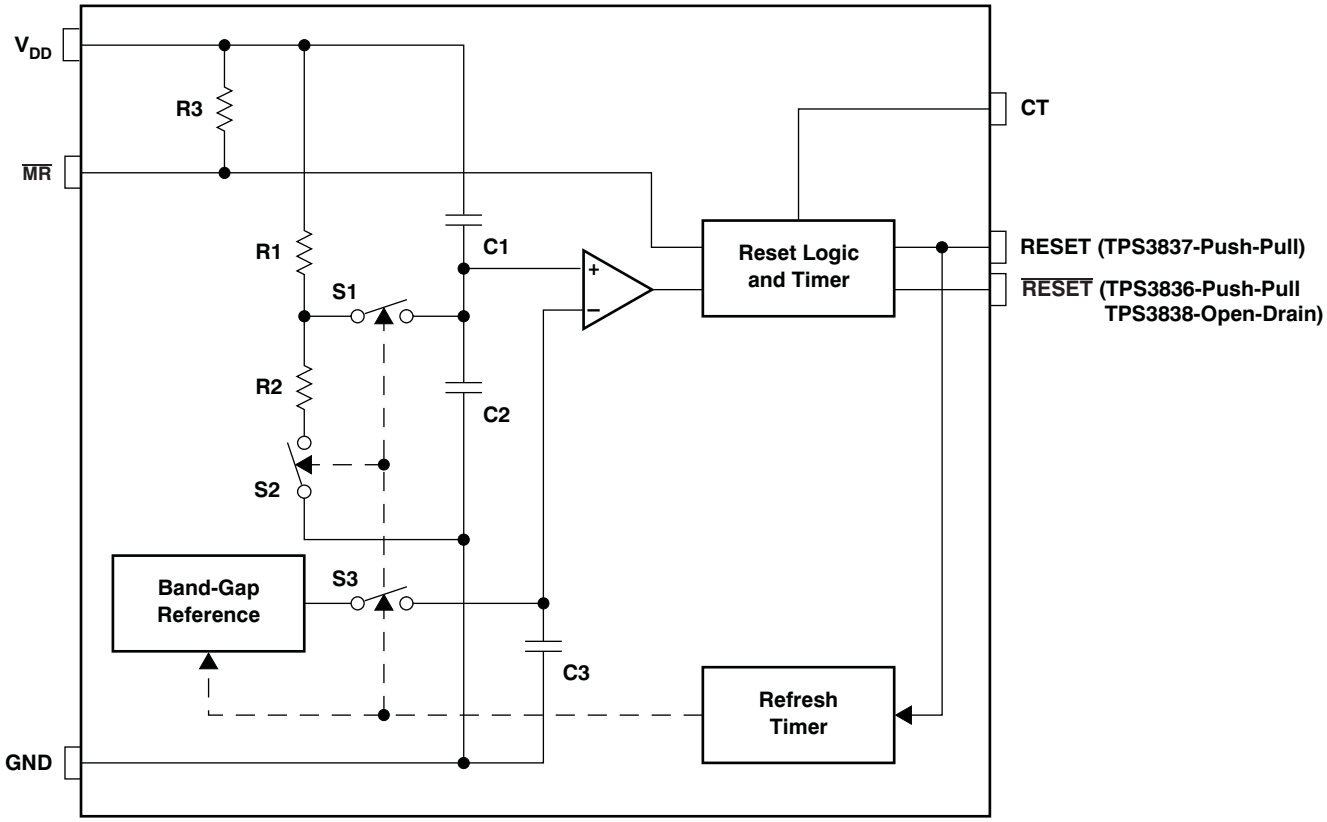
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_D	Delay time		$V_{DD} \geq V_{IT}$ + 0.2 V, $\overline{MR}$ = 0.7 × V_{DD}, CT = GND, See Timing Diagram	5	10	15	ms
			$V_{DD} \geq V_{IT}$ + 0.2 V, $\overline{MR}$ = 0.7 × V_{DD}, CT = V_{DD}, See Timing Diagram	100	200	300	
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{RESET}$ delay (TPS3836, TPS3838)	$V_{IL} = V_{IT}$ – 0.2 V, $V_{IH} = V_{IT}$ + 0.2 V			10	µs
			V_{IL} = 1.6 V			50	
t_{PLH}	Propagation (delay) time, low-to-high-level output	V_{DD} to RESET delay (TPS3837)	$V_{IL} = V_{IT}$ – 0.2 V, $V_{IH} = V_{IT}$ + 0.2 V			10	µs
			V_{IL} = 1.6 V			50	
t_{PHL}	Propagation (delay) time, high-to-low-level output	$\overline{MR}$ to $\overline{RESET}$ delay (TPS3836, TPS3838)	$V_{DD} \geq V_{IT}$ + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IL} = 0.7 × V_{DD}			0.1	µs
t_{PLH}	Propagation (delay) time, low-to-high-level output	$\overline{MR}$ to RESET delay (TPS3837)	$V_{DD} \geq V_{IT}$ + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IL} = 0.7 × V_{DD}			0.1	µs

TIMING REQUIREMENTS

At T_A = +25°C, R_L = 1 MΩ, and C_L = 50 pF, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_W	Pulse width	at V_{DD}	$V_{IH} = V_{IT}$ + 0.2 V, $V_{IL} = V_{IT}$ – 0.2 V	6			µs
		at $\overline{MR}$	$V_{DD} \geq V_{IT}$ + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}	1			

FUNCTIONAL BLOCK DIAGRAM

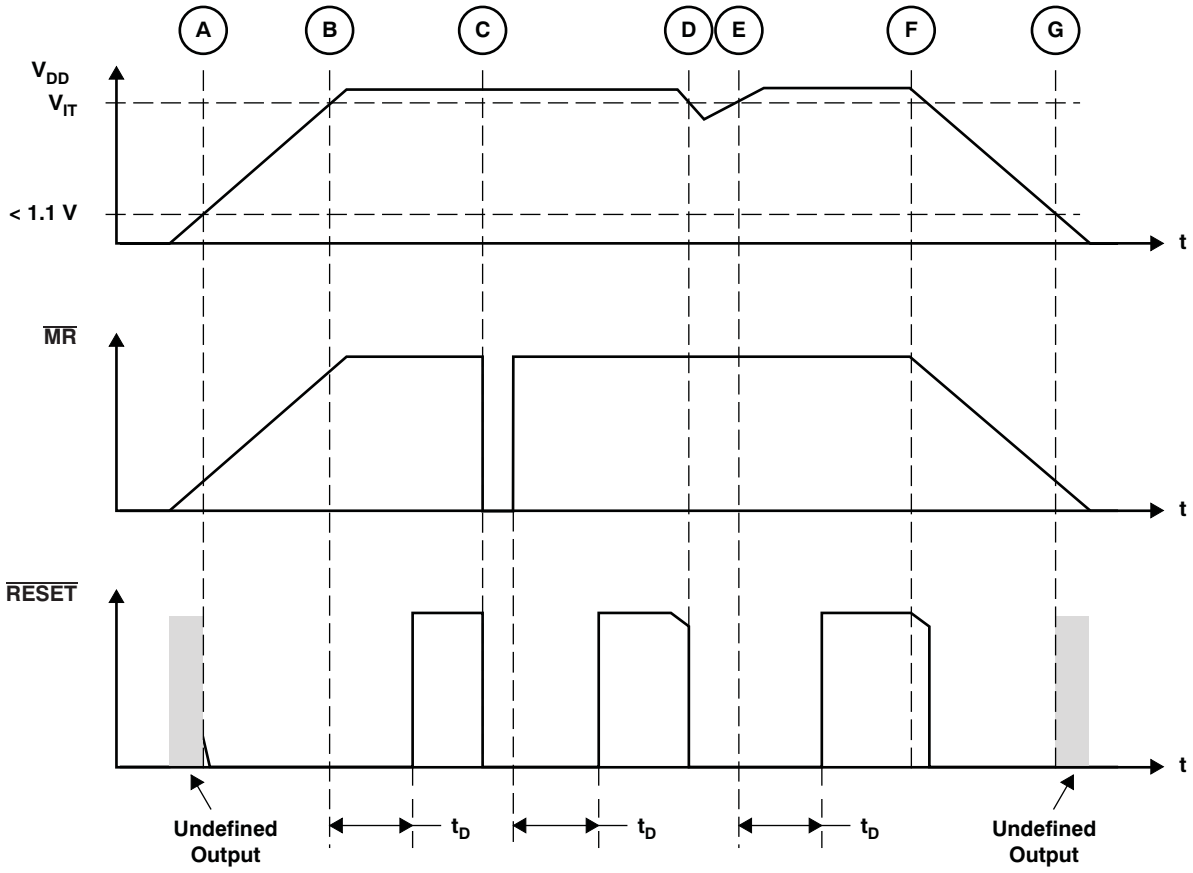


FUNCTION TABLE

$\overline{MR}$	$V_{DD} > V_{IT}$	$\overline{RESET}$ (1)	RESET (2)
L	0	L	H
L	1	L	H
H	0	L	H
H	1	H	L

(1) TPS3836 and TPS3838.
(2) TPS3837.

TIMING DIAGRAM



TYPICAL CHARACTERISTICS

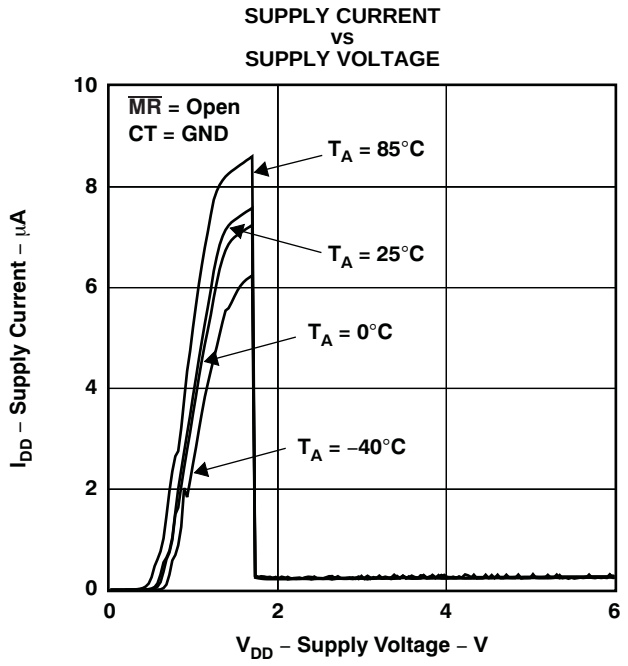


Figure 1.

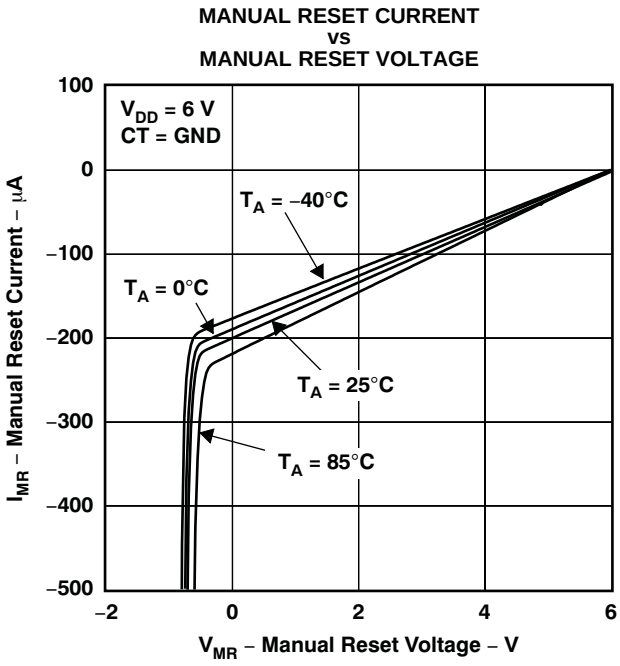


Figure 2.

TYPICAL CHARACTERISTICS (continued)

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

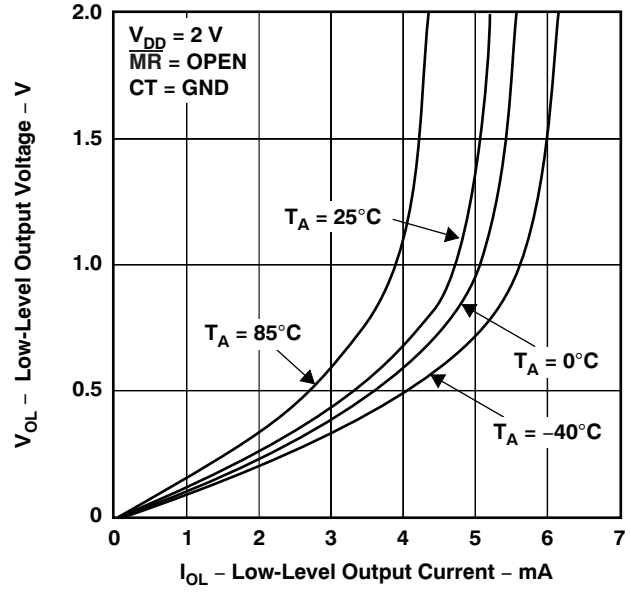


Figure 3.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

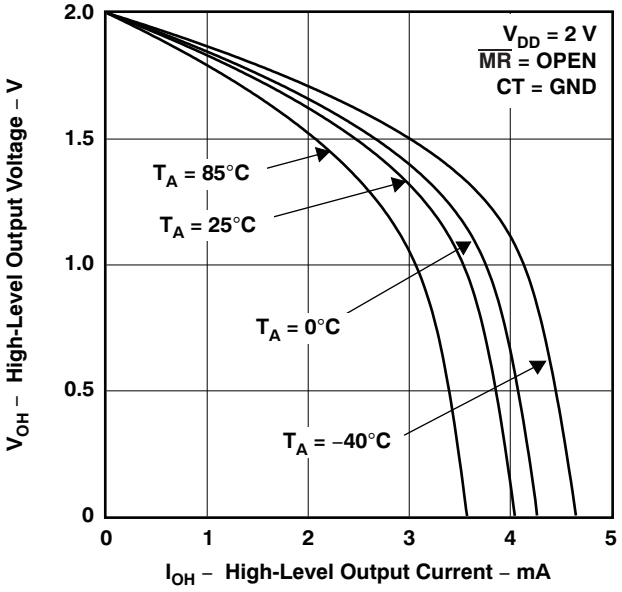


Figure 4.

NORMALIZED RESET THRESHOLD VOLTAGE
VS
FREE-AIR TEMPERATURE

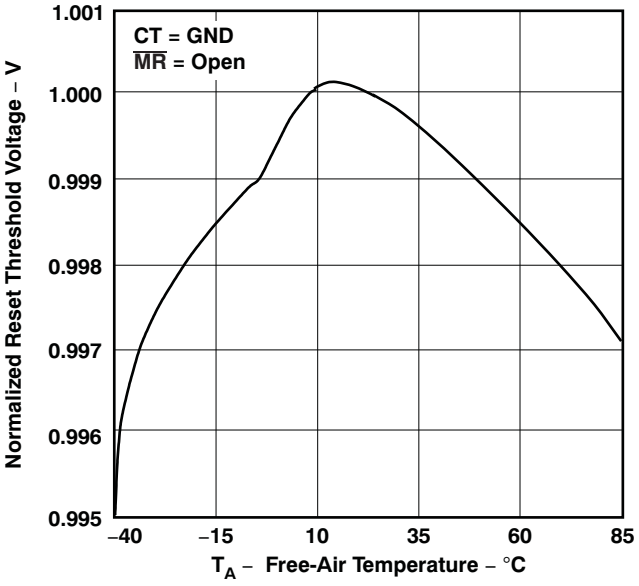


Figure 5.

MINIMUM PULSE DURATION AT V_{DD}
vs
V_{DD} THRESHOLD OVERDRIVE

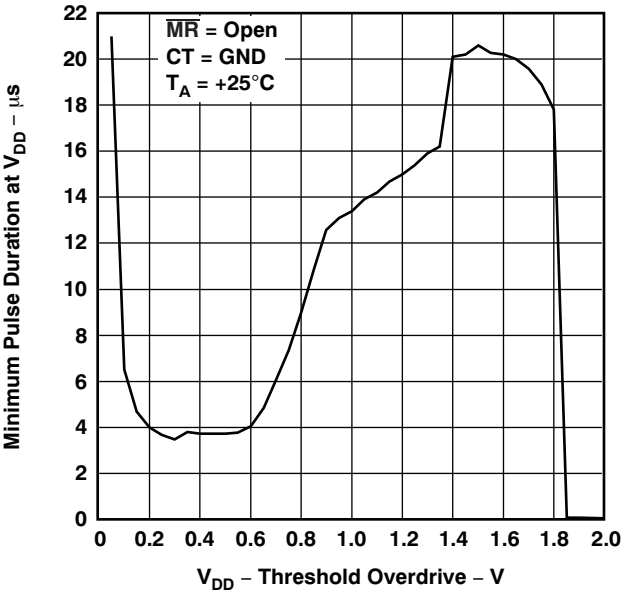


Figure 6.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS3836E18DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836E18DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836E18DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836E18DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836H30DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836H30DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836H30DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836H30DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836J25DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836J25DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836J25DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836J25DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836K33DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836K33DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836K33DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836K33DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836L30DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836L30DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836L30DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3836L30DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3837E18DBVRG4	ACTIVE	SOT-23	DBV	5		TBD	Call TI	Call TI
TPS3837E18DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3837E18DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3837J25DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3837J25DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS3837J25DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3837J25DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3837K33DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3837K33DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3837K33DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3837K33DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3837L30DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3837L30DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3837L30DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3837L30DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3838E18DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3838E18DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3838E18DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3838E18DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3838J25DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3838J25DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3838J25DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3838J25DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3838K33DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3838K33DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3838K33DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3838K33DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3838K33DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3838K33DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3838L30DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3838L30DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS3838L30DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3838L30DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

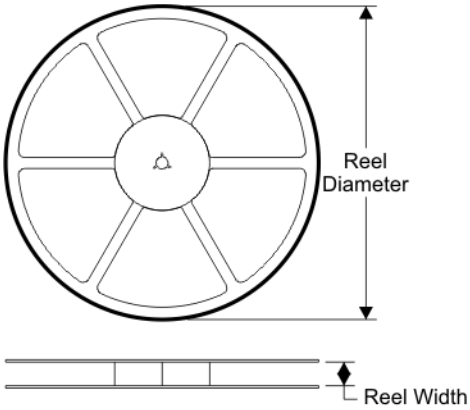
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

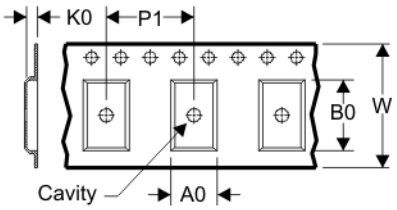
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

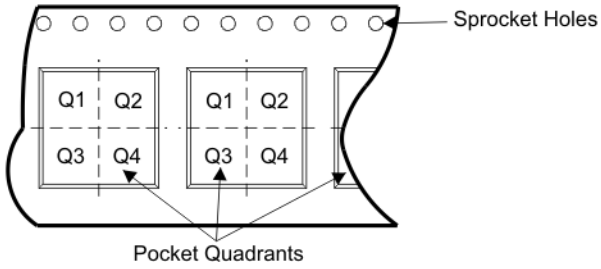


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

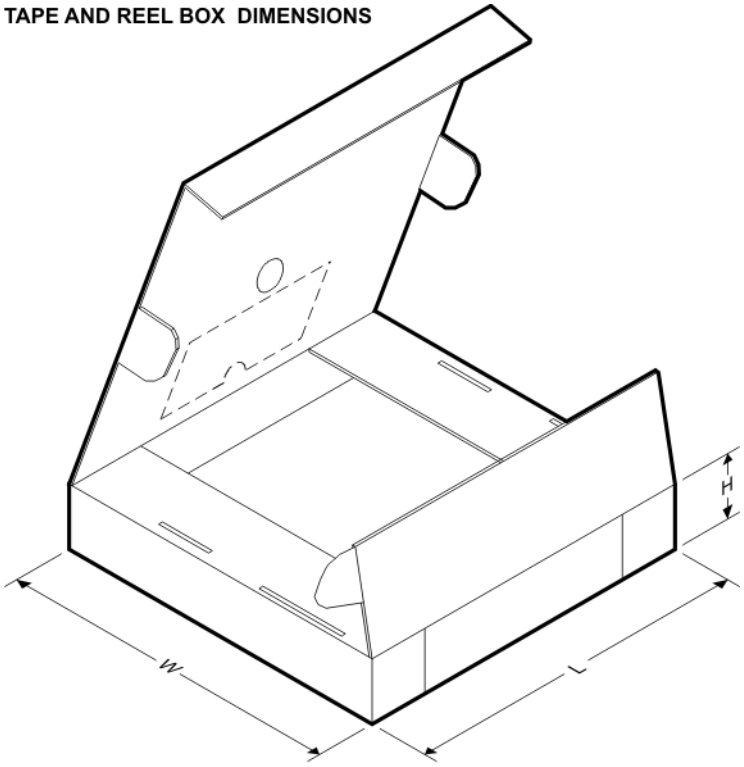
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3836E18DBVR	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3836E18DBVT	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3836H30DBVR	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3836H30DBVT	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3836J25DBVR	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3836J25DBVT	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3836K33DBVR	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3836K33DBVT	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3836L30DBVR	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3836L30DBVT	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3837E18DBVT	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3837J25DBVR	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3837J25DBVT	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3837K33DBVR	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3837K33DBVT	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3837L30DBVR	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3837L30DBVT	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3838E18DBVR	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3838E18DBVT	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3838J25DBVR	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3838J25DBVT	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3838K33DBVR	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3838K33DBVT	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3838L30DBVR	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3
TPS3838L30DBVT	DBV	5	SITE 40	180	9	3.15	3.2	1.4	4	8	Q3

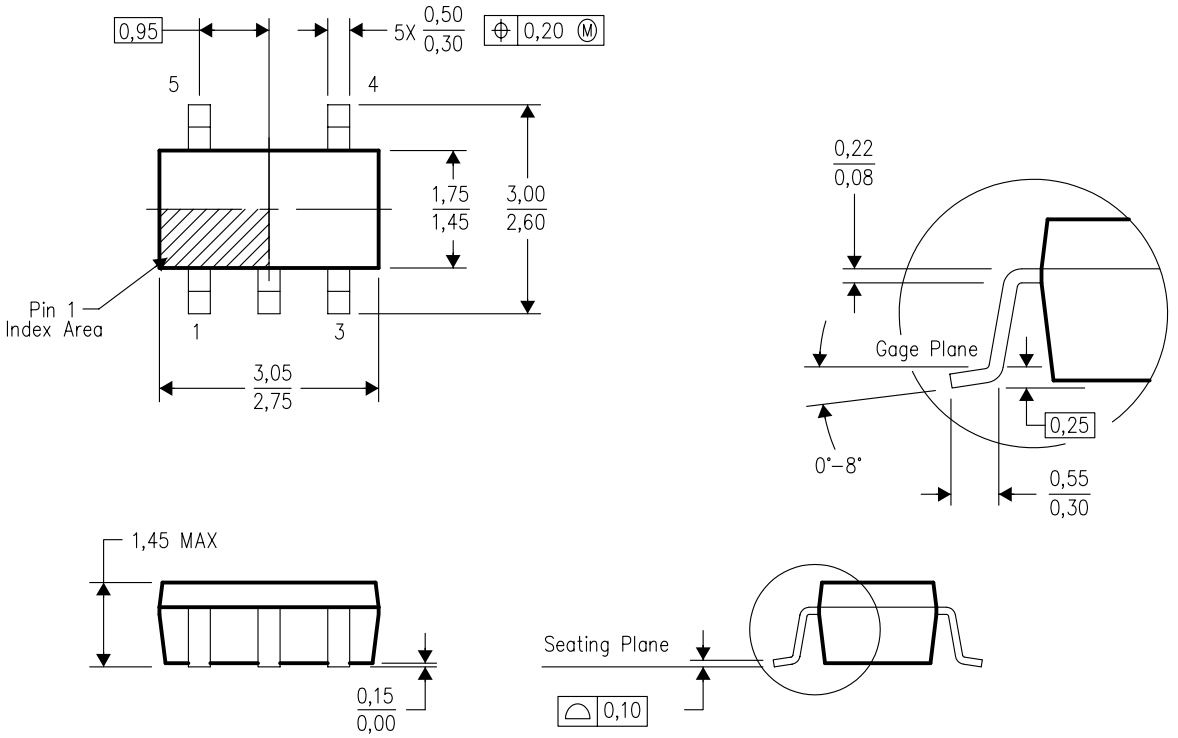
TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPS3836E18DBVR	DBV	5	SITE 40	182.0	182.0	0.0
TPS3836E18DBVT	DBV	5	SITE 40	182.0	182.0	0.0
TPS3836H30DBVR	DBV	5	SITE 40	182.0	182.0	0.0
TPS3836H30DBVT	DBV	5	SITE 40	182.0	182.0	0.0
TPS3836J25DBVR	DBV	5	SITE 40	182.0	182.0	0.0
TPS3836J25DBVT	DBV	5	SITE 40	182.0	182.0	0.0
TPS3836K33DBVR	DBV	5	SITE 40	182.0	182.0	0.0
TPS3836K33DBVT	DBV	5	SITE 40	182.0	182.0	0.0
TPS3836L30DBVR	DBV	5	SITE 40	182.0	182.0	0.0
TPS3836L30DBVT	DBV	5	SITE 40	182.0	182.0	0.0
TPS3837E18DBVT	DBV	5	SITE 40	182.0	182.0	0.0

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPS3837J25DBVR	DBV	5	SITE 40	182.0	182.0	0.0
TPS3837J25DBVT	DBV	5	SITE 40	182.0	182.0	0.0
TPS3837K33DBVR	DBV	5	SITE 40	182.0	182.0	0.0
TPS3837K33DBVT	DBV	5	SITE 40	182.0	182.0	0.0
TPS3837L30DBVR	DBV	5	SITE 40	182.0	182.0	0.0
TPS3837L30DBVT	DBV	5	SITE 40	182.0	182.0	0.0
TPS3838E18DBVR	DBV	5	SITE 40	182.0	182.0	0.0
TPS3838E18DBVT	DBV	5	SITE 40	182.0	182.0	0.0
TPS3838J25DBVR	DBV	5	SITE 40	182.0	182.0	0.0
TPS3838J25DBVT	DBV	5	SITE 40	182.0	182.0	0.0
TPS3838K33DBVR	DBV	5	SITE 40	182.0	182.0	0.0
TPS3838K33DBVT	DBV	5	SITE 40	182.0	182.0	0.0
TPS3838L30DBVR	DBV	5	SITE 40	182.0	182.0	0.0
TPS3838L30DBVT	DBV	5	SITE 40	182.0	182.0	0.0

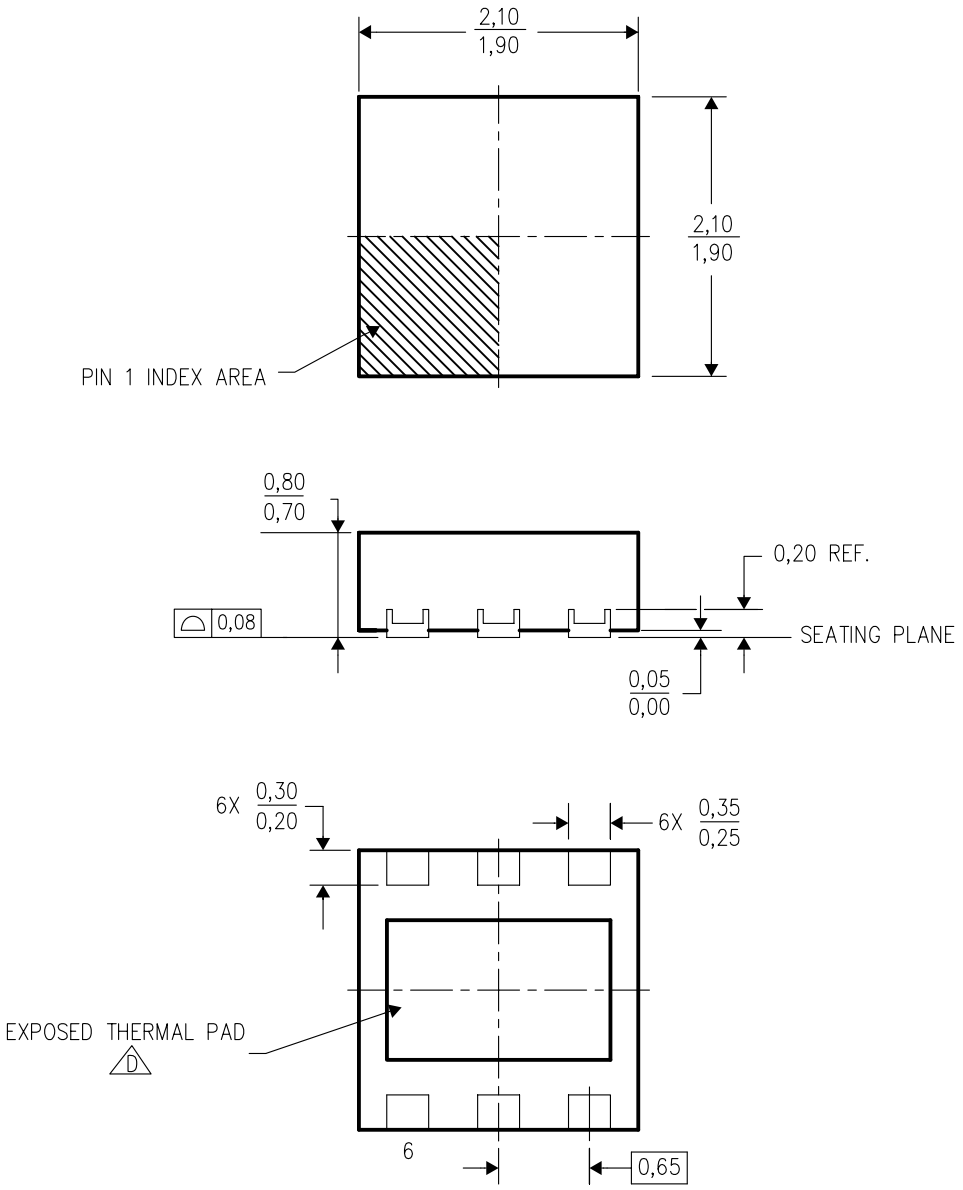
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DRV (S–PDSO–N6) PLASTIC SMALL OUTLINE



4206925/C 01/07

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

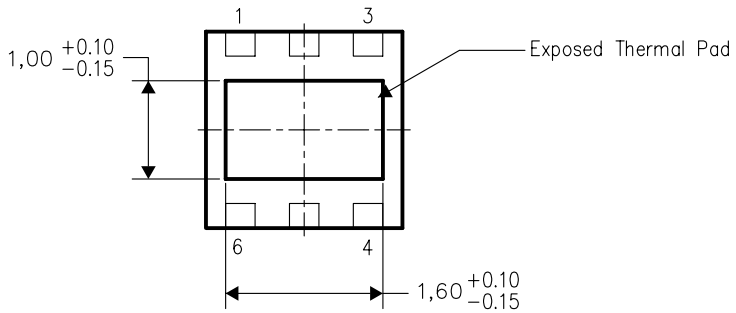
DRV (S–PDSO–N6)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

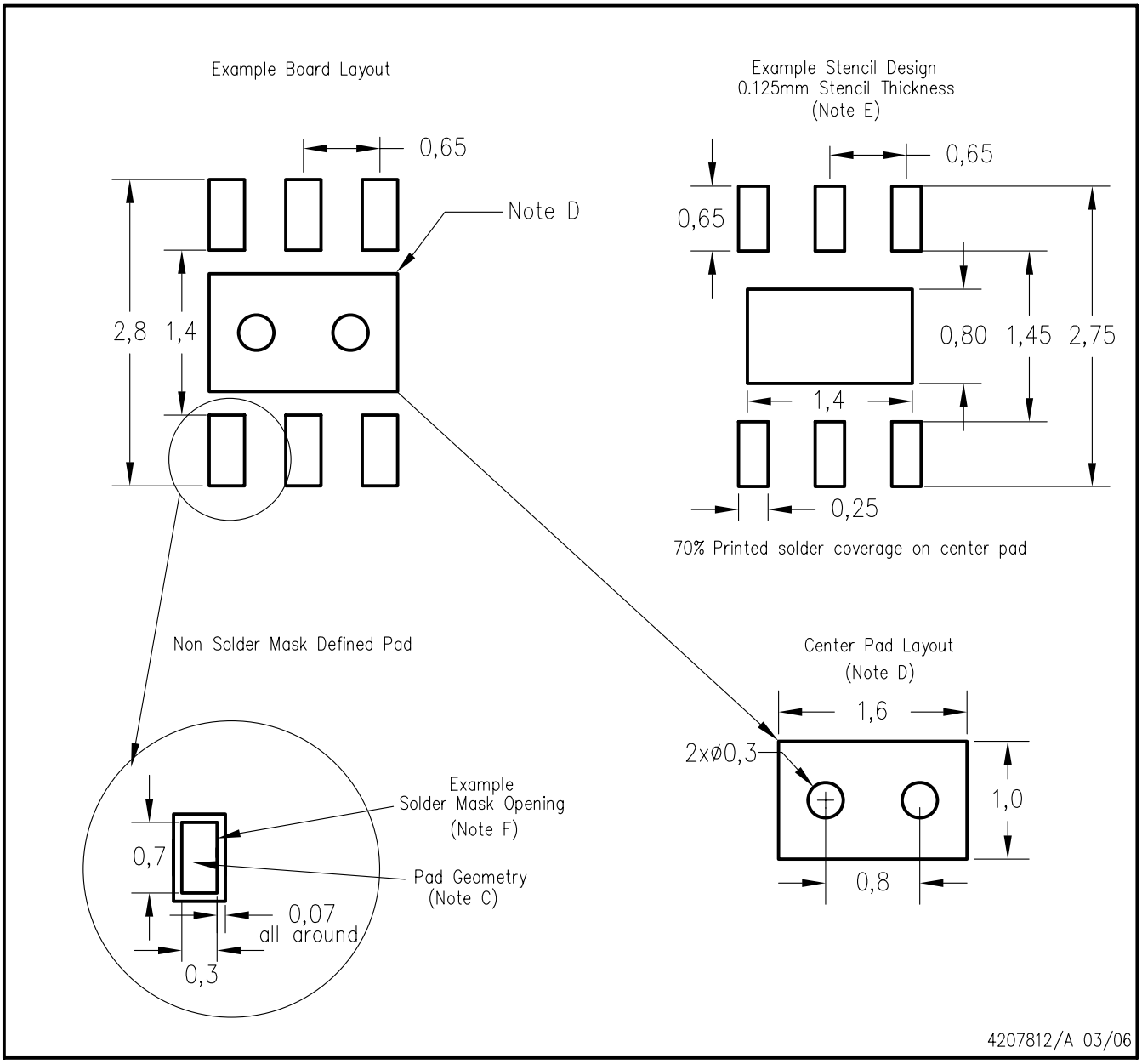


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRV (S–PDSO–N6)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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