To see the operation of the impedance matching network, a test bench configuration was constructed in Cadence, as shown in Figure 1. The top circuit simulations the antenna as a source, with the impedance matching network driving a load, R_{Load}, representing the power amplifier chip CC2591. Due to the manufacturer of the chip, Texas Instruments, not publishing the output parameters of their chip, the resistance is setup as a variable. The bottom circuit simulates the antenna and power amplifier without an impedance matching network.

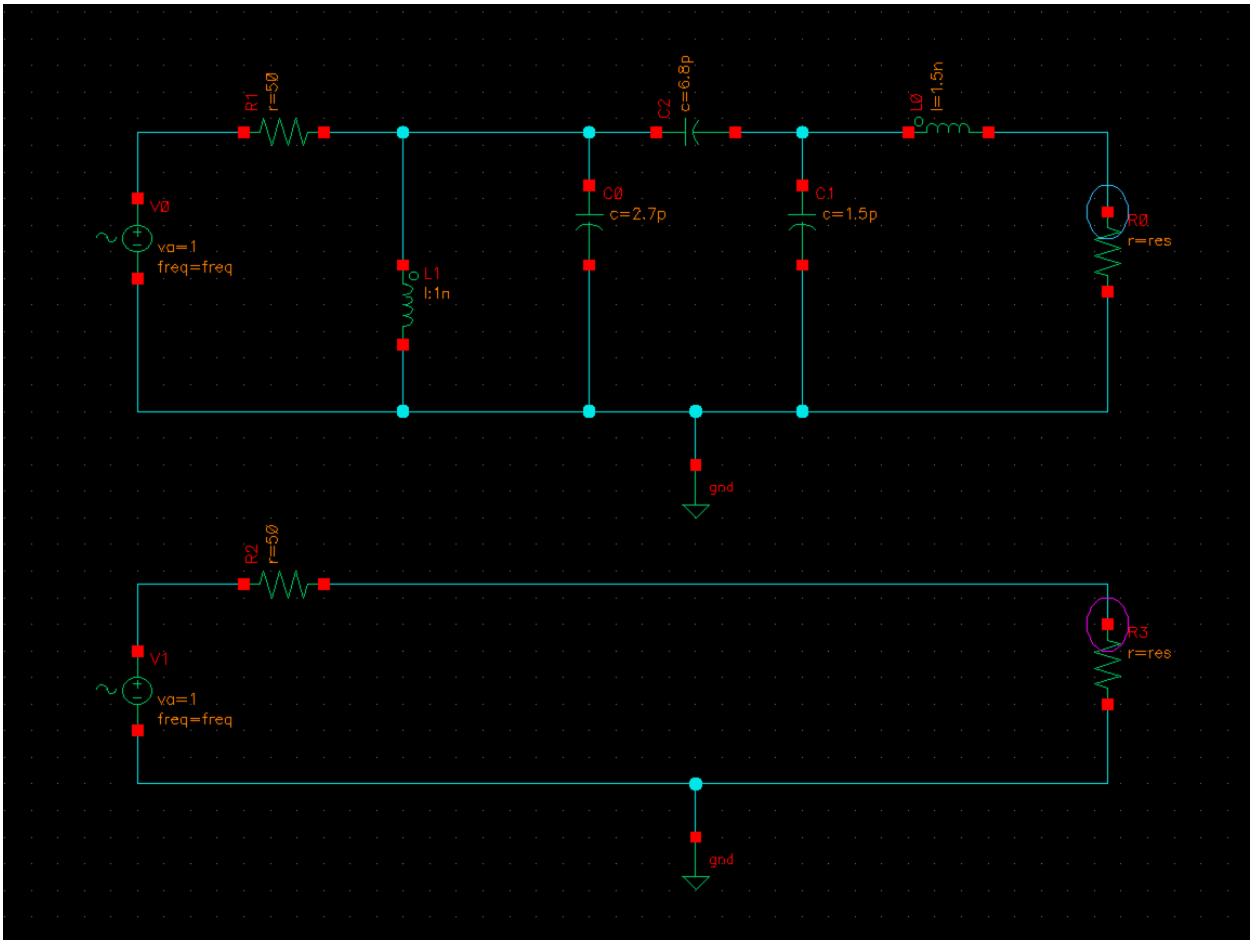

Figure 1 - Test bench showing schematic with impedance matching network and one without.

To see the frequency response of the utilized circuit, the sources in Figure 1 were swept from 1MHz to 100GHz, with the ratio of the output efficiencies, as calculated in Eq. 1, plotted versus frequency in Figure 2. This figure of merit shows the efficiency gain of the impedance matching circuit compared to that without the impedance matching circuit.

$$\frac{\eta_{z-match}}{\eta_{nom}} = \frac{P_{Out-Z}}{P_{In-Z}} \frac{P_{In-nom}}{P_{Out-nom}} \quad \textbf{(1)}$$

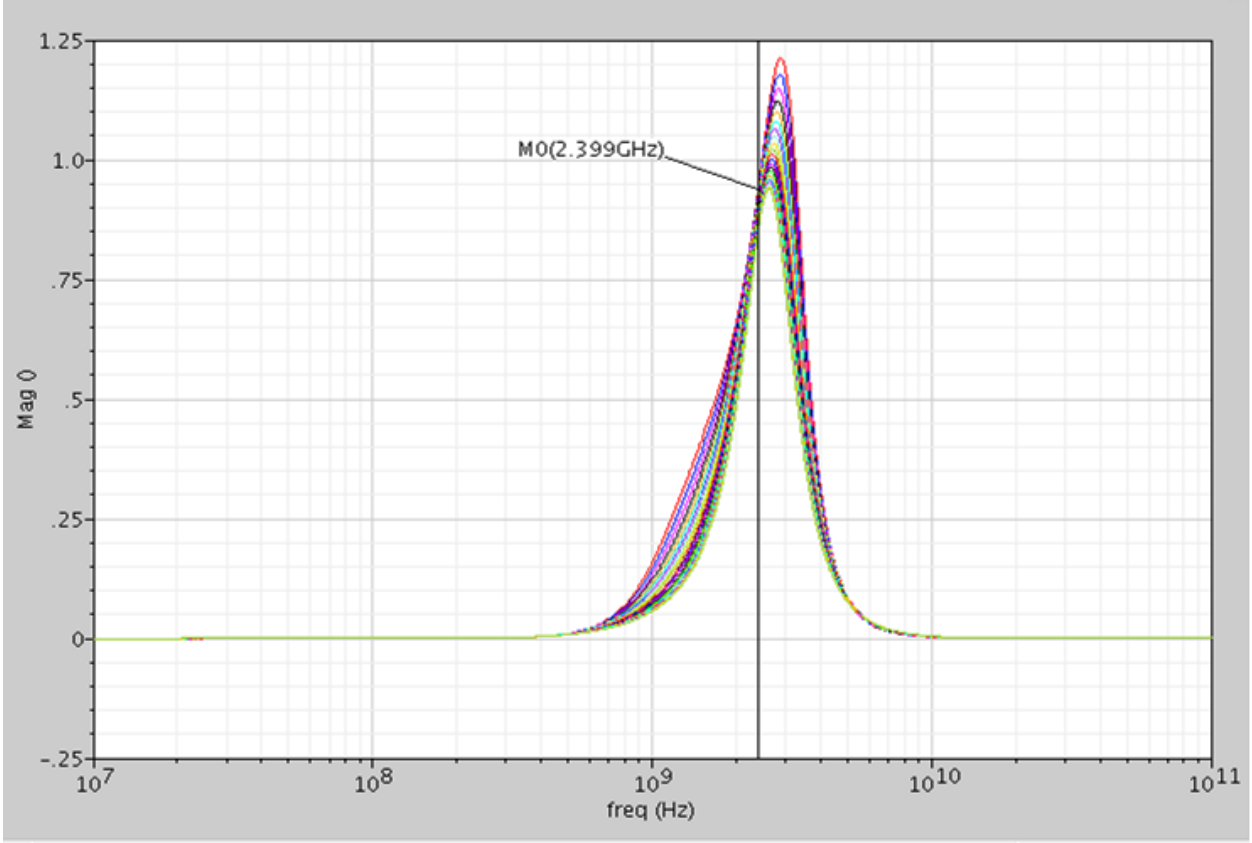

Figure 2 – Plot of Eq. 1 over frequency range from 1MHz to 100GHz with R_{Load} varied from 20Ω to 50Ω. The red line is 20Ω and the green line is 50Ω.

As seen in Figure 2, the value R_{Load} was swept from 20Ω to 50Ω. This choice of values came from the type of impedance matching network being analyzed. The given topology would only be used if the impedance looking into the power amplifier is less than that of the 50Ω antenna.

From Figure 2, it can be seen that the network is being used to filter out frequencies other than that in a narrow band, or a pass-band filter. In addition, slight gain might be achieved depending upon the impedance value of the power amplifier.