Theory of Operation

Circuit: DC/DC Buck Converter

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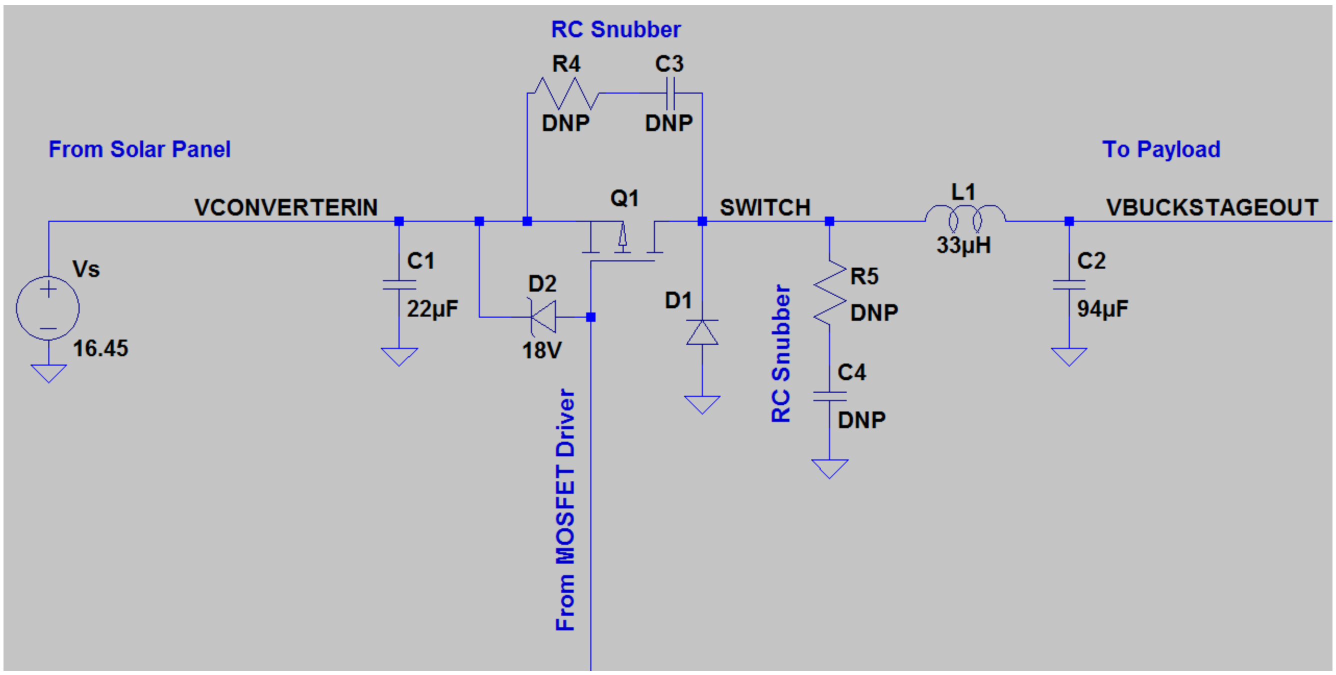

Figure 1: The step-down "buck" converter schematic with test circuitry used in simulations.

DC/DC "Buck" Converter Overview

The *Maximum Power Point Tracker* (MPPT) uses a DC/DC converter to perform the impedance conversion required to match the solar panel impedance with the load impedance, allowing the extraction of maximum power from the solar panel. Each solar array on the Fox-2 spacecraft will use seven Spectrolab *Ultra Triple Junction* (UTJ) solar cells in series producing maximum power at the minimum of 14.994V when the cells are operating at 60°C and at the maximum of 20.454V when the cells are at -60°C. This corresponds to a 5.46V swing in the maximum power point voltage, requiring a form of tracking. The specified 4.1V maximum MPPT output voltage will always be lower than the solar panel input voltage, therefore a DC/DC "buck" converter is appropriate to provide the step-down in voltage and the impedance match required as shown in **Figure 1**.

The buck converter is operated at a switching frequency of 250 kHz with a *Pulse-Width Modulated* (PWM) drive signal. Through hardware testing, a minimum load of 200 mA is required to remain in *Continuous Conduction Mode* (CCM). The output voltage PWM "Soft" limit provides the required feedback to protect the payload when high power is available from the panel but low power is required from the MPPT. Operation below 200 mA is achievable without adverse output voltage effects due to the output voltage limit even though the buck converter is in *Discontinuous Conduction Mode* (DCM). Lastly, the decision to implement a non-synchronous buck converter was made to decrease complexity of the prototype circuit at the expense of a large reduction of MPPT power conversion efficiency. This can be improved in future design revisions.

Due to the uncommon method of feedback method used for the output voltage PWM limit and virtually no feedback during maximum power point regulation, the component values derived with the standard buck converter voltage regulator equations were not appropriate. The voltage regulator equations from SLVA477[1] provided component values that were vastly underestimated from the implemented values used to allowed proper operation which were realized during board bring-up. This document will first cover the calculation of the buck converter component values based on Texas Instruments application note SLVA477, and then the analysis of the implemented buck converter will be presented.

DC/DC Buck Converter Calculations

The equations used to calculate the component values used in the buck converter were obtained from Texas Instruments SLVA477. The application note assumed that a regulated output voltage was the intended function. The equations were modified to provide the maximum calculated inductance and capacitance possible with normal operation. The output voltage is allowed to swing between 3.3V and 4.1V. An optimum switching frequency of 300 kHz was also used.

Equation 1 is used to predict the worst-case duty cycle present in the system assuming an efficiency of 85%:

$$D_{MAX}=\frac{V_{\mathrm{OUT}}\cdot\eta}{V_{\mathrm{IN(Min)}}}=\frac{(4.1\mathrm{V})\cdot(0.85)}{(14.994\mathrm{V})}=0.232 \quad \textbf{(1)}$$

Worst-case output current assuming conversion loss occurs at 3.3V output voltage and 6.154W output power as calculated in **Equation 2**. This is the maximum current that flows through inductor L1 during normal operations.

$$I_{\mathrm{MAX}}=\frac{P_{\mathrm{OUT}}}{V_{\mathrm{OUT}}}=\frac{6.154\,W}{3.3\mathrm{V}}=1.501\mathrm{A} \quad \textbf{(2)}$$

The ripple current was then estimated as 30% of the maximum current the inductor will conduct as shown in **Equation 3**.

$$\Delta I_{L}=0.3\cdot I_{\mathrm{OUT(max)}}=0.3\cdot 1.501\mathrm{A}=0.450\mathrm{A} \quad \textbf{(3)}$$

Equation 4 was used to calculate the inductor L1 value based on the estimated ripple current. The equation values were used to maximize the required inductance due to the lack of output voltage regulation:

$$L_{\mathrm{MIN}}=\frac{V_{\mathrm{OUT}}\cdot(V_{\mathrm{IN(max)}}-V_{\mathrm{OUT}})}{\Delta I_{L}\cdot F_{S}\cdot V_{\mathrm{IN}}}=\frac{4.1\mathrm{V}\cdot(20.454\mathrm{V}-4.1\mathrm{V})}{0.450\mathrm{A}\cdot 300\mathrm{kHz}\cdot 20.454\mathrm{V}}=24.28\,\mu H \quad \textbf{(4)}$$

Using **Equation 5**, the peak MOSFET Q1 and inductor L1 current can be calculated:

$$I_{\mathrm{SW(max)}}=\frac{\Delta I_{L}}{2}+I_{OUT(max)}=\frac{0.450\mathrm{A}}{2}+1.865\mathrm{A}=2.09\mathrm{A} \quad \textbf{(5)}$$

1 SLVA477 (PDF) – Basic Calculation of a Buck Converter's Power Stage

According to the CDBA340L-G datasheet, diode D1 has a maximum forward voltage drop of 400 mV and can handle an average forward current of 3A. The average forward current through D1 is calculated in **Equation 6:**

$$I_F = I_{OUT(max)} \cdot (1 - D) = 1.501\text{A} \cdot (1 - 0.232) = 1.153\text{A} \tag{6}$$

Following **Equation 7**, the power dissipated in D1 due to the forward voltage drop was calculated as:

$$P_D = I_F \cdot V_F = 1.153\text{A} \cdot 0.400\text{V} = 0.461\text{W} \tag{7}$$

The output capacitor was selected to limit the output voltage ripple to within about 1% peak to peak. **Equation 8** shows the calculated output capacitance required for 1% ripple:

$$C_{\text{OUT(min)}} = \frac{\Delta I_L}{8 \cdot f_S \cdot \Delta V_{OUT}} = \frac{0.450\text{A}}{8 \cdot 300\text{KHz} \cdot 0.041\text{V}} = 4.57\text{uF} \tag{8}$$

C1	**µF**	4.7
C2	**µF**	4.57
L1	**µH**	24.28
D1	**V_F**	0.4
D2	**V_Z**	18
Q1	**$R_{DS(ON)}$**	0.08

Table 1: Component values calculated and used for the buck converter design.

DC/DC Buck Converter Analysis

The measured conversion efficiency for the MPPT DC/DC circuit is about 80%. Actual device values implemented in the circuit include the ZXMP4A57E6 for MOSFET Q1, CDBA340L-G for diode D1, BZX384-B18 for diode D2, and an ELL-CTV180M from Panasonic for inductor L1. The maximum duty cycle the buck converter will operate at has been calculated in **Equation 9**:

$$D_{MAX} = \frac{V_{\text{OUT}} \cdot \eta}{V_{\text{IN(Min)}}} = \frac{(4.1\text{V}) \cdot (0.8)}{(14.994\text{V})} = 0.219 \tag{9}$$

Since the inductance value is known and so is the switching frequency, the inductor ripple current can be calculated with reasonable accuracy. **Equation 10** was used to calculate the inductor ripple current in the operational circuit.

$$\Delta I_L = \frac{(V_{\text{IN(max)}} - V_{OUT}) \cdot D}{f_S \cdot L} = \frac{(20.454\,V - 4.1\text{V}) \cdot 0.219}{250\,kHz \cdot 33\,\mu H} = 0.434\text{A} \tag{10}$$

The maximum current that flows through inductor L1 during normal operations with 80% efficiency, is:

$$I_{\text{MAX}} = \frac{P_{\text{OUT}}}{V_{\text{OUT}}} = \frac{5.792\,W}{4.1\text{V}} = 1.413\text{A} \tag{11}$$

Using **Equation 11**, the peak MOSFET Q1 and inductor L1 current can be calculated as shown in **Equation 12**:

$$I_{\mathrm{SW(max)}} = \frac{\Delta I_L}{2} + I_{OUT(max)} = \frac{0.434\,A}{2} + 1.413\mathrm{A} = 1.63\mathrm{A} \qquad \textbf{(12)}$$

The value of L1 required to support the ripple current calculated in **Equation 10** is calculated in **Equation 13,** and represents the absolute minimum inductance required to support the ripple current with 80% conversion efficiency. Effectively, the ripple current incorporates the conversion efficiency into the inductance calculation.

$$L = \frac{V_{\mathrm{OUT}} \cdot \left(V_{\mathrm{IN(max)}} - V_{\mathrm{OUT}}\right)}{\Delta I_L \cdot F_S \cdot V_{\mathrm{IN}}} = \frac{4.1\mathrm{V} \cdot (20.454\mathrm{V} - 4.1\mathrm{V})}{0.434\mathrm{A} \cdot 250\mathrm{kHz} \cdot 20.454\mathrm{V}} = 30.213\,\mu H \qquad \textbf{(13)}$$

Again, diode D1 according to the CDBA340L-G datasheet has a maximum forward voltage drop of 400 mV, and can handle an average forward current of 3A. The average forward current through D1 is:

$$I_F = I_{OUT(max)} \cdot (1 - D) = 1.413\mathrm{A} \cdot (1 - 0.219) = 1.104\mathrm{A} \qquad \textbf{(14)}$$

Following **Equation 15** the power dissipated in D1 due to the forward voltage drop can also be calculated:

$$P_D = I_F \cdot V_F = 1.104\mathrm{A} \cdot 0.400\mathrm{V} = 0.442\mathrm{W} \qquad \textbf{(15)}$$

The output capacitor was selected to limit the output ripple to within about 100 mV peak to peak. The observed ripple voltage in reality is much higher than the calculated ripple. It is theorized that the lack of output feedback increases the observed ripple voltage. This could be evaluated more in further study. **Equation 16** shows the calculated output ripple voltage with the implemented output capacitance.

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \cdot f_S \cdot C_{\mathrm{OUT(min)}}} = \frac{0.434\mathrm{A}}{8 \cdot 250\mathrm{kHz} \cdot 94\,\mu F} = 2.3\mathrm{mV} \qquad \textbf{(16)}$$

C1	**µF**	22
C2	**µF**	94
L1	**µH**	33
D1	**V_F**	0.4
D2	**V_Z**	18
Q1	**$R_{DS(ON)}$**	0.08

Table 2: Component values as used on the MPPT board.