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May 8, 2014

MPPT Future Work

Current Status and Issues:

As reported in the technical paper, the reportable efficiency of the electrical system at the end of MSD II was 47%. The circuit that achieved this efficiency was only prototyped on a breadboard and is reported in the schematic attached. The eagle files can be found under the SVN repository under "web\public\Design\Electronics\BOARD DESIGN\Eagle\TE Board (Eagle) - MOSFET" Note: that only the schematic here is correct. The board actually ordered with the GaN FET design is found under the TE Board (Eagle) folder. One board error not listed in the paper obviously has been corrected in the MOSFET Eagle revision. (This error was the PMOS (Q2) footprint/layout was actually flipped and the drain and source pins were flipped)

The major problems with the circuit leading to this inefficiency can be attributed to 3 main things: power dissipation due to diode forward voltage drop, active drive circuit power dissipation, and "switching losses." The first two are somewhat obvious; the diode power dissipates power because it has a forward voltage drop around .4 Volts and passes a large current when it is on. The active gate drive circuit was only meant as a simple prototype solution to high side PMOS gate drive. Power will be dissipated upon charging the gate of the high side FET, but power will also be dissipated when the gate is discharged at a rate of $\sim V_{in}^2/R_{gate}$. For fast gate charge, this resistor needs to be small. However, this results in a larger power dissipation in the discharge phase as related in the above equation. The last major aspect will be discussed in more detail.

As shown in Figure 1, one gate drive solution tried was charging and discharging using a high power (high output current) op-amp. The problem with this is as seen in Figure 1, since high current is required to charge power MOSFETs and therefore power op-amp's would be required, the op-amp themselves have a slow charge rate. This is known as slew rate in the data sheet.

For “large” enough op-amps, the slew rate from 0-20V is typically on the order of 1us, which is very slow. Again, see Figure 1 to view this effect.

Figure 1: Gate charge using high power op-amp

Figure 2: RLC Ringing noticed at the gate of the PMOS switch

Another issue in driving the gate of a power MOSFET is the effect shown in Figure 2. This seems to be the result of some RLC ringing. Note: that the gate voltage spiked up to 60V! This effect is due to charging the gate very quickly; allowing transients induced through the transistor as it tries to turn off to effect the gate voltage. To prevent this, one could use a snubber circuit. This should allow the ringing to filter out and greatly increase efficiency. Alternatively, if a different regulator could be used with multiple outputs, an isolated supply could be used to drive the gates, removing the previous RLC drive effects. See the article by Boonyaroonate for an example of this. An effective gate drive circuit is paramount for the design and unfortunately, gate drive circuits for high side PMOS are rarely found on the internet. Some simple circuits can be implemented, but these transient effects will be encountered and will be key in designing an efficient converter. High current gate charging is required, while transients need to be filtered out. Remember: These effects also change with switching frequency! Choosing a low switching frequency will likely make driving easier, however, component size and inductor losses will be larger.

Possible Solutions and Ways forward:

Option 1: Choose different converter design

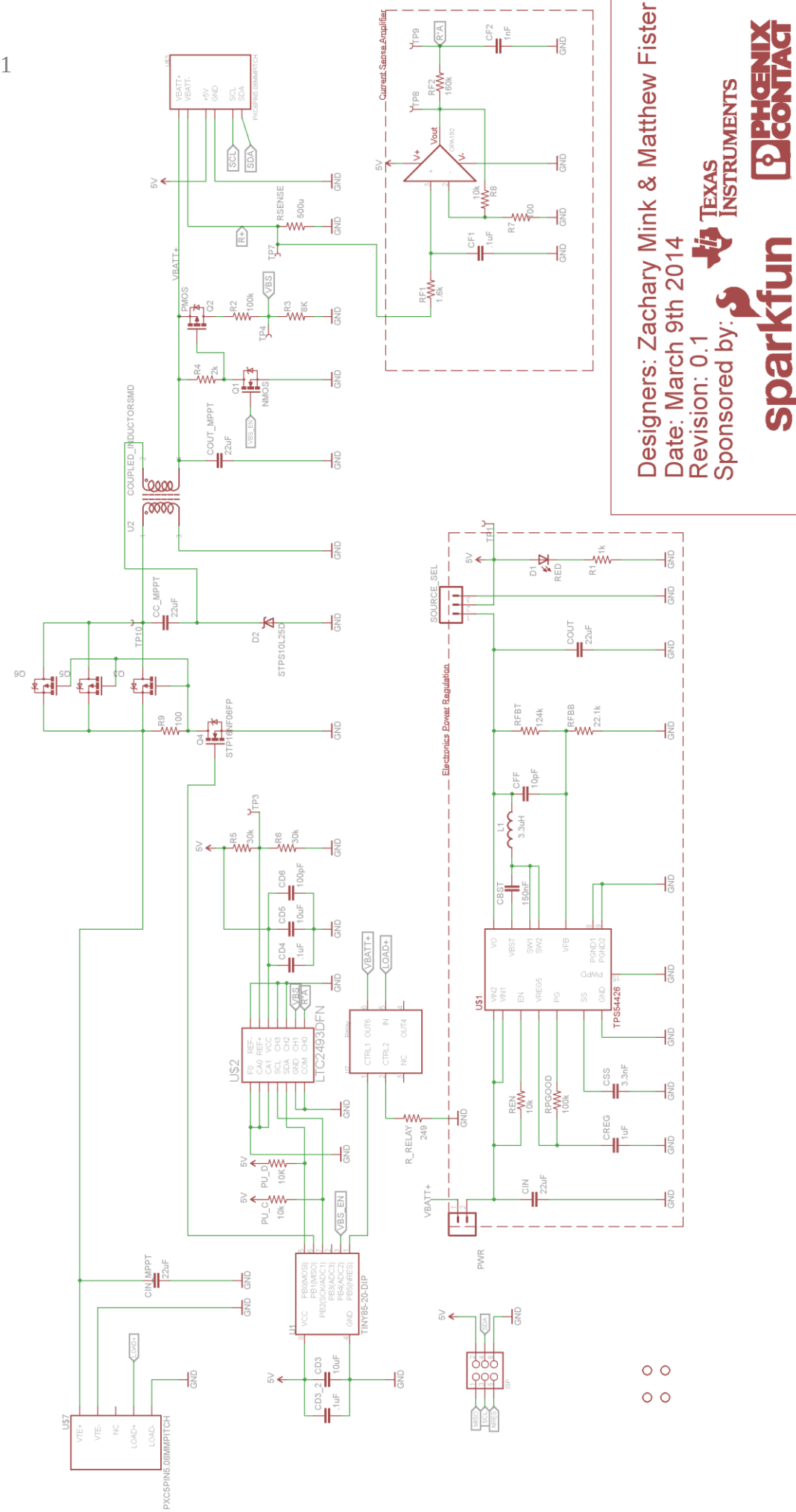
For the obvious advantage of having at least marginally efficient converter, a different topology could be considered. Many converter designs are available, though some have been specifically designed and tested for MPPT with thermoelectrics. The most important resource that should be covered specifically is "Development of a thermoelectric battery-charger with micro controller-based maximum power point tracking technique" by Eakburanawat and Boonyaroonate. They provide detailed schematics with components values and the chips they used.

The main advantage of changing converter topologies is the support and documentation involved as well as technical support available within the EE department for other topologies. The SEPIC more specifically has an easily driven low side switch for example that would make the drive circuitry fairly straight forward. However, the switching frequency and therefore the gate capacitance and transient/frequency response of the circuit have to be taken into account when designing the drive circuitry. The switching devices should also be chosen such that the breakdown voltages will not be exceeded including under transients which may reach much higher voltages than expected given inductance and capacitance of DC-DC converters.

Option 2: Improve upon ZETA

To improve upon the original ZETA converter, the previously mentioned aspects should be analyzed. The gate drive circuit would be a place to start. An alternative to the PMOS design is to find or design a bootstrap circuit for a high side NMOS. Utilizing an NMOS should reduce the on resistance and should yield a marginal increase in efficiency. The other device that could be

changed would be the diode. Doing some research to replacing this would be useful, however, some ideas would be replacing the diode with a PMOS transistor. Then, possibly using a negative supply voltage from a multiple output regulator could allow the PMOS to turn on given the constant zero/GND voltage. Another possible solution would be to use a coupled inductor to reverse a +5 input to a -5 gate voltage on the transistor. This would result in much smaller switching frequencies possible though. The advantage of the ZETA converter is in its lower capacitance requirements. This requires high switching frequencies though! With much smaller inductors and ceramic caps, if the ZETA is tuned correctly, the overall efficiency should be quite high as compared to an equivalent buck-boost or SEPIC.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Date: March 9th 2014
Revision: 0.1
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