Agenda Items

1. **Status Update**
   a. **Mechanical Subsystem**
   Completed the re-design of the enclosure for the extruded version. Awaiting feedback on the design. Once feedback is received, we can carry out the heat analysis to determine whether the enclosure will be able to dissipate all the heat. If not, will have to re-evaluate some placement of heat sinks to help. Need to decide if we are going to try and build this enclosure or just a model of it of some sorts. Also if really needed the heat analysis can be carried out without feedback and be done by tonight. Last time we talked we were having two FPGA's creating about 9 W of heat each, the hard drive tray producing about 2 W.

   Alonso - Responsible for carrying out the heat analysis of the enclosure and helping Matt with detailed drawings of individual components. I will be away from Wednesday night until Sunday morning for a conference, but will be available to work on anything remotely.
   Matt - Responsible for detailed drawings of components along with Alonso.

   b. **FPGA Board Subsystem**
   As of now the work on the FPGA schematic has been put on hold so the software development can begin. The FPGA dev kit boards are all that are needed to complete the demo so the schematics are lowest priority.

   c. **CXP HSMC Subsystem**
   Steve Brown is currently working on the CXP HSMC PCB layout working from where Lennard left off.

   d. **Software Subsystem**
   Three dev kits were purchased by D3 to use during the rest of our project. As of now all three have been turned on and visually inspected. A "Hello World" demo has been completed to prove the ARM core is functioning properly. The software tasks were split into three parts and each were assigned to a group member.

   Jordan - Responsible for Qsys to integrate the SoC and the FPGA. Many of the busses and registers will need to be mapped from the FPGA to the SoC so the SoC can dynamically adjust the characteristics of the FPGA. There are references to overall designs of Qsys systems, but we will need to develop a custom mapping of the Qsys signals.

Lennard - Responsible for overall Verilog architecture and

Kyle - Responsible for ARM core communication with FPGA. This part will consist of booting up the hard processor, establishing connection with FPGA, and sending commands from the ARM core to FPGA. The ARM core will be responsible for controlling the FPGA functions ”on the fly” while processes on the FPGA are running.

As of now most of the work has been a group effort to get the basic parts of the FPGA setup. This includes getting QSYS files setup, system files setup, and to get everything else setup to match the D3 setup.

2. **Action Items for week 11/3/2014 - 11/10/2014**
    a. **Mechanical Action Items:**
        i. Mechanical Design Review 11/6/2014
    b. **Hardware Action Items:**
        i. Status Update from D3 on CXP HSMC PCB layout
    c. **Software Action Items:**
        i. Complete System File
        ii. Complete QSYS setup
        iii. Work with Steve to get an understanding of the next steps
    d. **Other Action Items:**
        i. Update Project Plan
        ii. Continue working on Final Presentation
        iii. Continue working on Final Technical Paper
        iv. Update EDGE with new material