Analysis of thermoelectric cooler performance for high power electronic packages

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A B S T R A C T

In this paper, an analysis of thermoelectric cooler (TEC) performance is conducted for high power electronic packages such as processors. Based on the TEC module parameters, two sets of analytical solutions for TECs in system constraints are derived for the junction temperature $T_j$ at a fixed cooling power $Q_c$, and for $Q_c$ at a fixed $T_j$, respectively. As against the iterative procedure often reported in literature, the major advantage of the present analytical method lies in the fact that the solutions can be obtained without resorting to the pellet thermoelectric parameters and geometric details. Two cooling scenarios, the processor test and the processor cooling under end-user conditions, are analyzed based on the present analysis models for two commercial TECs with high cooling power capacities nominal. Analytical results show that significant thermal enhancements are achievable based on optimized currents and cooling configurations. The validation of the present analysis is also conducted through experimental measurements and comparison with previous solutions.

1. Introduction

High power electronic packages like processors have posed great thermal management challenges in either manufacturing processes or end-user operations. According to the international technology roadmap for semiconductors [1], the projected maximum testing power in the coming decade is 300 W and above per device under test (DUT) for both client and server processors. The end-user maximum power dissipations are projected to be 140 W and 198 W for the cost-performance and high performance electronics, respectively. The adoption of multiple cores on the silicon die has once mitigated the heat flux on the die, but ultimately the power, driven by electrical performance and multi-functional-ity, would doom to go up again, resulting in increasing thermal management challenges. Since conventional air cooling techniques for high power electronic packages are reaching the limits in term of cooling capacity, various efforts have been devoted to enhance the cooling design and performance [2–13]. Among them, the use of thermoelectric coolers (TECs), in combination with air cooling or liquid cooling approaches, is gaining more and more attention. The major thermal benefit of this development trend lies in the fact that a negative temperature gradient and thus reduced thermal resistance could be generated from the use of TEC. Compact in size and silent in operation, the TEC is easy to be integrated into a server or desktop computer system in comparison with the vapor compression cooling technology [9]. In the design and development of TEC apparatus, it is crucial to establish effective methodology to determine and optimize the TEC performance within the cooling system constraints. The mostly used approach is the iterative method as is given in [9,12]. This method offers results based on TEC pellet thermoelectric properties, which is nonetheless tedious and time-consuming for designers to use in practice. Presented in [13] are some semi-analytical solutions for the $T_j$ optimization associated with the operation current and pellet geometry. It is noted that these semi-analytical expressions contain inter-dependent parameters such as $\Delta T$ and $T_c$, which essentially requires an iterative procedure for full closure. Simons and his co-workers derived analytical solutions for electronics modules based on Mathcad [2,3]. They concluded that TEC coolers were not suitable for high power multi-chip modules based on available TECs then. It is noted that their solution expressions were not simplified to concise form, and the usage was limited to the same group of authors. All the above mentioned predictive methods require prior knowledge of TEC pellet geometrical dimensions and thermoelectric properties including Seebeck coefficient, thermal conductivity, and electrical resistivity. These properties vary with TEC manufacturing processes, and, as manufacturers’ proprietary information, are mostly not available to designers. A detailed discussion on the material properties variation versus carrier concentration and composition can be found in [14]. In addition, the optimization study on the TEC operational parameters such as electrical current is still limited for TEC cooling under various manufacturing and users’ conditions. Verification of TEC analysis methodology and cooling performance across different researchers are also rarely reported.
In this paper, analytical expressions based on TEC module parameters are developed to analyze TEC thermal performances in processor cooling conditions. Two sets of analytical expressions for TECs are derived to obtain the junction temperature \( T_j \) at a fixed cooling power \( Q_c \) and the cooling power \( Q_c \) at a fixed \( T_j \). The solutions can be obtained in a straightforward manner without the iterative procedure and prior knowledge of detailed pellet dimensions and thermoelectric properties. Two representative application scenarios for the thermal management of processors are investigated based on the present analysis methodology. In the first application, the TEC is used to conduct processor test at lowered temperatures, in which shortened test time is targeted at elevating power. In the second scenario, the TEC is used to cool down the processor with a fixed power for the end-user operation, and reduced junction temperature and improved electrical performance are targeted through TEC operational optimization. Comparison with previous work is also conducted for cross- verifications of the present analysis tool.

### 2. TEC thermal balance equations

Our analysis starts with the basic one-dimensional thermal balance equations of the TECs, which are available in previous literature such as [9,11,12,14]. It is noted that the temperature effect on the thermoelectric properties, the effects of ceramic plates, and joining copper traces and electrical contact resistances, which are negligibly small, are not included in the present thermal balance model.

Cooling power absorbed at the TEC cold side:

\[
Q_c = 2N \left( s f T_c - \frac{I^2 \rho}{2G} - k G \Delta T \right)
\]  

(1)

Electrically driven TEC power:

\[
Q_{te} = 2N \left( s f \Delta T + \frac{I^2 \rho}{2G} \right)
\]  

(2)

Total heat generated at the hot side of TEC:

\[
Q_h = Q_c + Q_{te} = 2N \left( s f T_h + \frac{I^2 \rho}{2G} - k G \Delta T \right)
\]  

(3)

TEC temperature differential \( \Delta T \):

\[
\Delta T = T_h - T_c
\]  

(4)

### Nomenclature

- \( \text{COP} \): coefficient of performance
- \( G \): geometry factor, defined by the ratio of area over length (m)
- \( I \): electrical current (A)
- \( k \): thermal conductivity (W/mK)
- \( K_m \): TEC module thermal conductance (W/K)
- \( N \): number of TEC thermocouples
- \( Q_c \): heat load (W)
- \( Q_{te} \): electrically driven TEC power (W)
- \( R \): thermal resistance (K/W)
- \( R_{ha} \): TEC hot side to ambient thermal resistance (K/W)
- \( R_{jc} \): junction to TEC cold side thermal resistance (K/W)
- \( R_m \): TEC module electrical resistance (Ohm)
- \( s \): Seebeck coefficient (V/K)
- \( S_m \): TEC module Seebeck coefficient (V/K)
- \( T \): temperature (K or °C)
- \( T_{ha} \): TEC hot side temperature in supplier’s datasheet (K or °C)
- \( V \): voltage (V)
- \( Z \): figure of merit (1/K)

### Greek Letters

- \( D \): thermal interface material
- \( D_T \): TEC hot side to cold side temperature difference (K)
- \( G \): electrical resistivity (Ohm m)
- \( h \): thermal conductivity (W/mK)
- \( \rho \): electrical resistivity (Ohm m)
- \( \Delta T \): TEC hot side to cold side temperature difference (K)

### Subscripts

- \( c \): TEC cold side
- \( h \): TEC hot side
- \( ha \): TEC hot side to ambient
- \( j \): junction
- \( j c \): junction to TEC cold side
- \( m \): TEC module
- \( \text{max} \): maximum of given quantity
- \( \text{op} \): optimum
- \( \text{tim} \): thermal interface material

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**Fig. 1.** Schematic of the processor test configuration with a TEC and a liquid-cooled heat sink, together with the corresponding one-dimensional thermal resistance network.

A TEC enhanced cooling configuration is constrained by the thermal resistances at both the cold side and hot side. Here, two application scenarios mostly encountered for processor packages are schematically exemplified in Figs. 1 and 2, respectively. The first scenario simulates the processor testing in burn-in and system-level testing (SLT) applications. The thermal design task is to minimize the junction temperature and ambient temperature are fixed in advance. Such type of testing is required for each processor before its release to market. The second case (Fig. 2) simulates the processor cooling under user conditions. The power generation from processor is known and the design task is to minimize the junction temperature to the lowest level through TEC enhanced air cooling or liquid cooling techniques. The design and selection criteria are the lowest junction temperature with the TEC enhancement. The one-dimensional thermal resistance network for both application scenarios has been shown in Fig. 1. At the device side,

\[
T_j = T_c + Q_c R_{jc}
\]  

(5)

Thermal resistance correlation at the heat sink side is written as:
Fig. 1. Schematic of the TEC cooling of a processor with an air cooled heat sink at the top.

\[ T_h = T_a + (Q_{te} + Q_s)R_{ha} \]  

(6)

It is noted that all the thermal interface resistances are already absorbed in the lumped thermal resistance \( R_{jc} \) and \( R_{ha} \). TEC is referred as module electric resistance, \( R_m \), and \( R_{m} \) is the top.

There are eight unknown variables in Eqs. (1)–(7): \( T_h, T_c, \Delta T, Q_s, Q_{te}, T_a, Z \), given the known TEC parameters like \( \alpha, \rho, k \) and \( G \) are difficult to obtain directly from TEC manufacturers, who are inclined to protect their proprietary manufacturing materials and processes. To make the TEC cooling optimization feasible in the design and development stage, a new analysis method is proposed, so that the thermal balance equations for the TEC can be transformed in terms of the TEC module parameters. The module parameters \( S_m, R_m, \) and \( K_m \) are given in the following correlations:

\[ R_m = \frac{2N\rho}{G} \]  

(10a)

\[ K_m = 2NkG \]  

(10b)

\[ S_m = 2N \]  

(10c)

Here, \( R_m, K_m \), and \( S_m \) are denoted as module electric resistance, thermal conductance, and Seebeck coefficient, respectively. Based on the modular parameters, Eqs. (1)–(3) and (7) can be recast into the following form:

\[ Q_c = S_m I_c - \frac{R_m I_c^2}{2} - K_m \Delta T \]  

(11)

\[ Q_{te} = S_m I_c \Delta T + \frac{R_m I_c^2}{2} \]  

(12)

\[ Q_h = S_m I_c T_h + \frac{R_m I_c^2}{2} - K_m \Delta T \]  

(13)

\[ Z = \frac{S_m^2}{R_m K_m} \]  

(14)

Correspondingly, Eq. (8) is rewritten as follows:

\[ V = S_m \Delta T + R_m I \]  

(15)

At this stage, the TEC thermal balance equations in terms of the module parameters are closed with known module parameters and operational current. The module parameters, \( S_m, R_m, \) and \( K_m \) are obtainable with TEC specification parameters such as \( I_{max}, Q_{max}, \Delta T_{max}, T_s, \) and \( V_{max} \) which are usually given in supplier’s product datasheet. Here, \( \Delta T_{max} \) is the largest temperature difference obtainable between the hot and the cold ceramic plates at a given high side temperature \( T_{h0} \). \( I_{max} \) is the input current that can produce the maximum \( \Delta T_{max} \) across a TEC module, \( V_{max} \) is the DC voltage at the temperature difference of \( \Delta T_{max} \) at \( I = I_{max} \) and \( Q_{max} \) is the maximum amount of heat absorbed at the TEC cold side at \( I = I_{max} \) and \( \Delta T = 0 \). The following equations correlate the module parameters with the product specifications [15], namely,

\[ R_m = \frac{(T_{h0} - \Delta T_{max})V_{max}}{I_{max} T_{h0}} \]  

(16a)

\[ K_m = \frac{(T_{h0} - \Delta T_{max})V_{max} I_{max}}{2T_{h0} \Delta T_{max}} \]  

(16b)

\[ S_m = \frac{V_{max}}{T_{h0}} \]  

(16c)

Here, \( V_{max}, I_{max}, \Delta T_{max}, I_{max} \) are employed to calculate the module parameters. Luo [16] presented another method to calculate the parameters involving \( Q_{max} \) instead of \( V_{max} \), which would give virtually the same results, if not exactly the same. Based on Eqs. (4)–(6) and Eqs. (12)–(14), the optimization can be carried out even without knowing the parameters of specific TEC pellet geometrical details and thermoelectric properties. On the other hand, the geometrical optimization can be conducted through Eqs. (10a)–(10c) if the pellet properties such as \( N, s, \alpha, \rho, k \) and geometry factor \( G \) are known.

The analytical expressions for \( Q_c, \Delta T, T_h, \) and \( T_c \) are derived in the following equations. Care should be taken in the derivation to avoid errors and missing terms.

\[ Q_c(T_j, I) = \left( \frac{S_m^2 R_{ha}^2 - S_m I - K_m}{K_m} \right) T_j + K_m T_s + R_m I^2 \left( \frac{K_m R_{ha}}{2} - \frac{S_m R_{ha}}{2} + \frac{S_m R_{ha} I}{2} \right) \]  

\[ \Delta T(T_j, I) = \frac{(S_m R_{ha} I - 1) T_j + (T_s + S_m R_{ha} I) T_a + R_m R_{ha} I^2 \left( \frac{S_m R_{ha}}{2} - \frac{K_m R_{ha}}{2} + \frac{S_m R_{ha} I}{2} \right) \} {K_m (R_{jc} + R_{ha}) - (S_m R_{ha} I - 1) (S_m R_{ha} I + 1)} \]  

\[ T_h(T_j, I) = \frac{K_m R_{ha} T_a + (T_s + S_m R_{ha} I) T_j + R_m R_{ha} I^2 \left( \frac{S_m R_{ha}}{2} - \frac{K_m R_{ha}}{2} + \frac{S_m R_{ha} I}{2} \right) \} {K_m (R_{jc} + R_{ha}) - (S_m R_{ha} I - 1) (S_m R_{ha} I + 1)} \]  

\[ T_c(T_j, I) = \frac{(S_m R_{ha} I - K_m R_{ha} - 1) T_j + K_m R_{ha} T_a + R_m R_{ha} I^2 \left( \frac{S_m R_{ha}}{2} - \frac{K_m R_{ha}}{2} + \frac{S_m R_{ha} I}{2} \right) \} {K_m (R_{jc} + R_{ha}) - (S_m R_{ha} I - 1) (S_m R_{ha} I + 1)} \]  

\[ T_s(T_j, I) = \frac{S_m R_{ha} I - K_m R_{ha} - 1) T_j + K_m R_{ha} T_a + R_m R_{ha} I^2 \left( \frac{S_m R_{ha}}{2} - \frac{K_m R_{ha}}{2} + \frac{S_m R_{ha} I}{2} \right) \} {K_m (R_{jc} + R_{ha}) - (S_m R_{ha} I - 1) (S_m R_{ha} I + 1)} \]  

\[ T_c(T_j, I) = \frac{(S_m R_{ha} I - K_m R_{ha} - 1) T_j + K_m R_{ha} T_a + R_m R_{ha} I^2 \left( \frac{S_m R_{ha}}{2} - \frac{K_m R_{ha}}{2} + \frac{S_m R_{ha} I}{2} \right) \} {K_m (R_{jc} + R_{ha}) - (S_m R_{ha} I - 1) (S_m R_{ha} I + 1)} \]  

\[ T_s(T_j, I) = \frac{(S_m R_{ha} I - K_m R_{ha} - 1) T_j + K_m R_{ha} T_a + R_m R_{ha} I^2 \left( \frac{S_m R_{ha}}{2} - \frac{K_m R_{ha}}{2} + \frac{S_m R_{ha} I}{2} \right) \} {K_m (R_{jc} + R_{ha}) - (S_m R_{ha} I - 1) (S_m R_{ha} I + 1)} \]  

\[ T_c(T_j, I) = \frac{(S_m R_{ha} I - K_m R_{ha} - 1) T_j + K_m R_{ha} T_a + R_m R_{ha} I^2 \left( \frac{S_m R_{ha}}{2} - \frac{K_m R_{ha}}{2} + \frac{S_m R_{ha} I}{2} \right) \} {K_m (R_{jc} + R_{ha}) - (S_m R_{ha} I - 1) (S_m R_{ha} I + 1)} \]  

\[ T_s(T_j, I) = \frac{(S_m R_{ha} I - K_m R_{ha} - 1) T_j + K_m R_{ha} T_a + R_m R_{ha} I^2 \left( \frac{S_m R_{ha}}{2} - \frac{K_m R_{ha}}{2} + \frac{S_m R_{ha} I}{2} \right) \} {K_m (R_{jc} + R_{ha}) - (S_m R_{ha} I - 1) (S_m R_{ha} I + 1)} \]
Let $R_{in}$, $R_c = 0$, Eq. (17c) reduces to $T_h = T_a$, Eq. (17d) reduces to $T_c = T_a$, Eq. (17a) reduces to Eq. (11), and Eq. (17b) reduces to $\Delta T = T_a - T_p$ which agrees with the physical intuition. The analytical expressions for $T_h$, $\Delta T$, $T_m$, and $T_c$ are derived in terms of known $Q_c$ and listed in Eqs. (18a–d).

$$T_h(Q_c, l) = \frac{(S_m R_{in} I - 1)(S_m R_{in} I + 1) - K_m (R_{in} + R_c) Q_c - K_m T_a - R_m T_e (K_m R_{in} - S_m R_{in} I + 1)}{S_m^2 R_{in} I^2 - S_m I - K_m}$$

$$\Delta T(Q_c, l) = \frac{(1 - S_m R_{in} I) Q_c - S_m T_a + R_m T_e (\frac{1}{S_m R_{in} I} - S_m I)}{S_m^2 R_{in} I^2 - S_m I - K_m}$$

$$T_m(Q_c, l) = -\frac{K_m R_{in} Q_c + (K_m + S_m I) T_a + R_m R_{in} I (K_m + \frac{1}{2} S_m I)}{S_m^2 R_{in} I^2 - S_m I - K_m}$$

$$T_c(Q_c, l) = \frac{(S_m R_{in} I - K_m R_{in} I - 1) Q_c - K_m T_a - R_m T_e (K_m R_{in} + \frac{1}{2} S_m R_{in} I)}{S_m^2 R_{in} I^2 - S_m I - K_m}$$

It is interesting to note that, if $Q_c$ and $l$ are specified for a certain TEC, the hot side and cold side temperatures can be obtained without the information of $R_c$ at the cold side according to Eqs. (18c–d). Let $R_{in}$, $R_c = 0$, again we obtain the results agreeable with simplified cases. The other quantities such as $Q_a$, $Q_b$ can be obtained based on Eq. (16) or Eq. (18), the detail of which is omitted here due to limited space. The present analytical expressions have been presented in concise form to facilitate better usage of the analytical solutions in engineering development applications without resorting to detailed pellet geometry and thermoelectric properties. The feasibility of the present analytical method is to be demonstrated in the two processor cooling scenarios in the following section.

4. Results and discussion

4.1. Processor test optimization ($Q_c$ maximization)

In typical processor testing, the processor temperature is required to be fixed at a set point during running of different software programs. The allowable processor power should be maximized in the design of the test system. Following the solution with a known $T_j$, the maximum $Q_c$ can be obtained by setting its derivative to zero with respect to the operation current, namely,

$$\frac{\partial Q_c(T_j, l)}{\partial l} \bigg|_{\text{fixed } T_j} = 0$$

This result is in a quartic equation with respect to $l$, which has two real roots and two conjugate roots. Only the positive real root is physically meaningful as the optimal operational current. Two types of TECs with high nominal cooling power are selected for performance analysis. Listed in Table 1 are the details of the TECs used in this work. TEC1 has a power dissipation of 330 W and TEC2 has a power dissipation of 223 W. Fig. 3 illustrates the acoustic image of TEC1 in planar view with the thermoelectric array through a Sonoscan Gen5 ultrasonic microscopy. The TEC pellet layout can be clearly visualized from the echo image but it is not possible to capture the pellet dimensions accurately due to interference from electrical traces. Analytical calculation is conducted for lidded processors to simulate desktop/server test applications. $R_e$ has been set to be 0.32 k/W based on in-house characterization, and $R_{in}$ has been set to be 0.05 k/W, representing liquid cooling condition. A lowered temperature $T_j = 10 ^{\circ}C$ is imposed. To avoid mathematical reducency, the optimum current is graphically illustrated by plotting the $Q_c$ versus $l$ based on the analytical solution in Eq. (14), as demonstrated in Fig. 4. It is indicated that a maximum $Q_c$ can be obtained at the $I_{op} = 14–16$ A for both TECs. Though TEC1 has a nominal cooling power almost 50% higher than TEC2, TEC1 shows only slightly better thermal performance than TEC2 in the processor test scenario at $T_j = 25 ^{\circ}C$ and $50 ^{\circ}C$, respectively.

![Fig. 3. Photograph of a TEC and corresponding C-mode acoustic image at 35 MHz.](image-url)
4.2. User condition optimization ($T_j$ minimization)

Under the user condition, a TEC can be sandwiched between the heat sink and the processor to bringing down $T_j$ in operation. By assuming a fixed processor power, the $T_j$ minimization optimization can be conducted by setting the derivative of $T_j$ with respect to $I$ to be zero. Namely,

$$\frac{\partial T_j}{\partial I} \bigg|_{Q_c \text{ fixed}} = 0$$

Again, the optimized current $I_{op}$ can be graphically obtained based on the plot of $T_j$ versus $I$. The operational parameters are obtained as follows. $R_c = 0.32$ K/W for the thermal resistance from junction to TEC cold side, $R_{ha} = 0.05$ K/W for the liquid cooling condition, and $R_{ha} = 0.18$ K/W for the air cooling condition; $Q_c = 50, 70, 100, 140$ W. In all the cases $T_a = 35$ °C has been imposed.

The $T_j$ results versus $I$ are listed in Fig. 5 for TEC1 and Fig. 6 for TEC2, respectively. Both air cooling and liquid cooling cases are considered. It is seen that, for air cooling, the minimum $T_j$ is obtained at optimal currents of 8–9 A for TEC1 and of 10–11 A for TEC2. However, for the liquid cooling, the operation can be implemented at a high current of 14–16 A near to $I_{max}$ for both TECs. Due to the high performance of liquid cooling technique, removal of the total heat with the liquid cooling is more efficient than the air cooling counterpart.

The corresponding COP results for TEC1 under air cooling and liquid cooling conditions at different power inputs are shown in Fig. 7. It is worthwhile to discuss the maximization of COP herein, which has long been confused with the optimization of system cooling performance. In the present $T_j$ minimization, the COP is
that, in the junction temperature range of interest from 35 to 90 °C, 
the TEC-enhanced cooling performance at optimized current is al-
ways better than that without TEC. This conclusion is drawn 
mainly due to the technological improvement on the performances 
of TEC, which has the nominal cooling capacity above 200 W. At 
a heating power below around 100 W ($T_j < 70$ °C), the TEC-enhanced 
air cooling performance is even better than the liquid cooling 
alone. Fig. 10 compares the thermal performances of the two TECs 
in this paper under air cooling and liquid cooling conditions. 
Though the nominal cooling power of TEC1 is around 1.5 times that 
of TEC2, our analysis shows that virtually there is little difference 
in the resulting power dissipation in the junction temperature 
range from 35 to 90 °C.

Thus far it has been demonstrated that enhanced cooling capacity 
can be achieved through TEC enhanced air cooling and liquid cooling

![Fig. 7. Plot of COP versus current $I$ for TEC1 at different cooling conditions.](image1)

![Fig. 8. Plot of air cooling and liquid cooling techniques with TEC1.](image2)

![Fig. 9. Plot of air cooling and liquid cooling techniques with TEC2.](image3)
techniques. Extensive application of TEC enhanced cooling in processor testing is also in progress. Reliability would also be a concern in the use of TEC as cooling enhancement means and has been addressed in references such as [11]. Nonetheless, the widespread use of TEC for thermal management of high power electronic packages like processors under user conditions remains limited. Extra cost arises from the introduction of TEC and corresponding operational power consumption. Despite this, an implementation of hybrid cooling through the use of TEC in combination with liquid cooling for high-end gaming computers has been demonstrated and reported in [17].

4.3. Comparison with previous studies

Firstly, the present analysis method is compared with the results in [3], where a four-chip IBM module was cooled by four TECs operated at $I_{\text{max}}$. With the same pellet thermoelectric parameters and $I = I_{\text{max}}$, we can reproduce the same data plot as Fig. 7 in [3] for both air cooling and liquid cooling with TECs. For example, the same intersecting temperature point of $T_j = 47^\circ C$ at 438 W is obtained here for the air cooled cases with and without TEC enhancement, below which the TEC-enhanced cooling performance excels the case without TEC.

Another comparison is carried out with the iterative methods mostly used in the literature. Specifically, Ref. [12] is used for comparison since all the TEC properties and thermal parameters were traceable therein. In their study, the thermal performances were iteratively determined based on temperature-dependent correlations. In the present study, the same thermal resistances as [12] are used, but the module parameters are derived from suppliers’ datasheet and listed in Table 1 at $T_0 = 25^\circ C$ and $50^\circ C$, respectively. In addition, the module parameters are linearly extrapolated and tabulated at $T_0 = 69^\circ C$. The computed $T_j$ values versus $I$ for all the three $T_0$ values are shown in Fig. 11. It is seen that the similar level of optimal current and cooling capacity are attainable in spite of different $T_0$. In comparison, the case $T_0 = 69^\circ C$ represented by the triangle symbol in Fig. 11 is the closest to the optimized result [12], at which $T_0 = 69^\circ C$ was obtained based on the iteration procedure. It is obvious that a slightly better accuracy is reachable by considering the effect of temperature at the TEC hot side. To summarize, the present analytical solutions are able to provide a fast prediction in the TEC performance prediction for design and implementation, without resorting to the iterative process and pellet-level details like dimensions and thermoelectric properties.

4.4. Experimental study

The experimental measurement was also conducted based on a processor test platform. The test platform consists of a motherboard to provide electrical connections to the device under test (DUT). Loaded on the DUT, the TEC1 (330 W) was sandwiched between a liquid-cooled heat sink and a heater plate with thermal grease filled at the thermal interfaces, as indicated in Fig. 1. A high-power lidded processor was used for the DUT with built-in thermal diode to record $T_j$. In each test, the TEC current was fixed and the processor power $Q_c$ was varied to obtain $T_j$ when the steady-state was reached. The plot of $Q_c$ versus $T_j$ was attained, which appeared linear in the test range and, thus, $Q_c$ at specified $T_j$ can be extracted. Fig. 12 shows a comparison of measured $Q_c$ results as against analysis results at $T_j = 25^\circ C$. It is seen that good agreement is achieved between measurements and analysis.
5. Conclusions

Starting from the TEC basic thermal models, analytical solutions in concise form are developed for TEC cooling. The main feature of the present analytical method is that it makes full use of the modular parameters $S_m$, $R_m$, and $K_m$ for design and development optimization without iterative procedure and prior knowledge of TEC pellet properties and dimensions. Optimized current can be directly obtained by illustrating the cooling power $Q_c$ or $T_j$ versus $I$ with the present analysis method. It is noted that optimizing other parameters such as TEC pellet geometry and system thermal resistances can also be conducted based on our current analysis method.

Two typical processor thermal management scenarios are examined based on the present analytical solutions, namely, processor testing scenario and user-condition cooling scenario. Optimization work is conducted for the two applications with commercial TECs of high nominal cooling capacity. For the processor test scenario, the processor temperature is fixed and the liquid cooling technique is assembled at the TEC hot side to remove the heat. Maximum cooling power is obtained at $I_{op}$ around 15 A for both TECs. In the processor end-user application scenario, both TEC enhanced air cooling and liquid cooling techniques are examined. The lowest junction temperatures are obtainable at the optimal currents 8–9 A for the air cooling case with TEC1 and optimal currents 14–16 A for the liquid cooling case with TEC2. Though COP can be maximized at a relatively low current, it is not an optimization criterion in the present cooling scenarios. Comparison of the present analytical models with previous work is also conducted and good agreement is achieved. Finally, the analytical results are compared with measurement in a test platform and good agreement at fixed processor test temperature.

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References