**Abstract**

The RIT Electric Vehicle Team is designing a new electric motorcycle, requiring a more capable battery management system (BMS). A new revision of the existing BMS was designed to meet the higher voltage requirements of the new battery pack, as well as more stringent safety requirements. The developed system was successfully field-tested on the current electric motorcycle, and is ready to be integrated onto the new motorcycle.

## Background

The RIT Electric Vehicle Team (EVT) is a student-run organization dedicated to promoting the viability of electric vehicles through real-world demonstrations of electric drivetrains. EVT's flagship project since 2013 has been REV1, a fully-electric superbike converted from a 2005 Kawasaki Ninja ZX6RR. The team has competed annually in a professional racing circuit at New Jersey Motorsports Park since July of 2015.

Starting in 2018, EVT began working on a new electric motorcycle, named REV2. EVT's goal is to compete with REV2 in the Pikes Peak International Hill Climb in June of 2019. The new bike will feature new and upgraded components, including a 400V liquid-cooled lithium-ion battery pack, an Emrax 268 axial synchronous electric motor, a Reinhart motor controller, and an in-house designed frame. In addition to these exciting features, EVT also elected to build a new battery management system (BMS) for REV2 which will also be compatible with REV1.

A BMS handles safety and performance related functions that are vital for a competitive electric vehicle (EV), not only in the racing world, but commercially as well. Various architectures have been used in the EV industry, often involving a single, centralized piece of hardware containing all of the necessary electronics. This is not an optimal approach for EVT, due to the compact and streamlined nature of motorcycles.

This project team, P18262, is comprised of electrical team members of EVT, tasked with designing a new, custom battery management system. The scope of our project is to design and validate the hardware electronics, with a full system test on REV1 serving as the metric to evaluate our success. Our team had to work closely with other EVT members, primarily with the firmware and battery teams, to ensure a smooth integration of the BMS into our vehicles.

## Motivation

A BMS generally handles several tasks, which relate to safety and performance. The primary functions are cell balancing and voltage measurement. The purpose of cell balancing is to keep the voltages and state of charge of individual cells nearly equal. The metrics measured by the BMS are individual cell voltages and temperatures. Lithium batteries can become volatile in the wrong conditions.If they are overcharged or get too hot, they can become dangerous. Poor operating conditions can reduce the lifetime of the battery, driving up cost.

Safety is the primary motivation behind a BMS, so the main stakeholder is the rider of EVT's vehicles. They trust that the bikes are safe so they can focus on winning the race. EVT as a whole is our second stakeholder. They entrust this team to design and build a product that brings EVT to the next level in engineering design. As one of the performance vehicle teams in the school, it is important that EVT represents RIT in a positive light by demonstrating well-engineered and safe motorcycles to the people and communities it interacts with. Therefore, RIT and the growing EV market and community has a stake in our success.

EVT has made previous iterations of a BMS for REV1.. Three revisions have been built, with the latest version being BMS 3.3. The primary limitation of BMS 3.3 was that it was not able to be used with REV2's 400V battery. It was also unnecessarily large and expensive, while also being computationally underpowered. BMS 3.3 was also plagued by hardware faults, causing difficulties with firmware development. BMS 3.3 was unreliable and unsafe, and as a result, was never fully operational or integrated on to REV1 during a race or test day.

Since BMS 4.0 had to perform many different functions, it was important for the team to keep track of the requirements to avoid making the mistakes of previous iterations. Table 1 shows the condensed list of Customer Requirements, with the key points highlighted.

Table 1: Customer Requirements (revised 3/25/2018)

| Customer Rqmt. # | Importance | Description | Comments/Status |
|---|---|---|---|
| CR1 | 1 | Must conform with current EVT firmware standards | All requirements met by Engineering Requirements |
| CR2 | 1 | Hardware must be able to fit within new battery packs | |
| **CR3** | **1** | **Must be able to funtion with full pack voltage of up to 500V** | |
| CR4 | 2 | Must estimate state of charge | |
| **CR5** | **1** | **Measure cell voltage** | |
| **CR6** | **1** | **Measure cell temperature** | |
| **CR7** | **1** | **Must communicate pack status to vehicle network** | |
| CR8 | 1 | Must be powered by LVSS or full pack | |
| CR9 | 2 | Must conform with current EVT safety standards | |
| **CR10** | **2** | **Must balance pack quickly** | |
| CR11 | 2 | Must be able to balance while pack is being charged | |
| CR12 | 2 | Must be manufacturable by EVT with available equipment | |
| CR13 | 3 | Must conform with EVT mounting standards | |
| CR14 | 3 | Must estimate state of health | |
| CR15 | 2 | Must have legacy support (REV1 battery packs) | |

Table 2 demonstrates the translation from the Customer Requirements to the Engineering Requirements. The Engineering Requirements give a qualitative and quantitative summary of the functions needed on BMS 4.0. Due to the high number of requirements, detailed traceability diagrams were made to keep the team on track.

Table 2: Engineering Requirements (revised 3/25/2018)

| Rqmt. # | Importance (1-5 : high-low) | Source (Customer Req#) | Function | Engr. Requirement (metric) | Unit of Measure | Marginal Value | Ideal Value |
|---|---|---|---|---|---|---|---|
| S1 | 1 | CR1 | Compliance/ Performance | Use STM F3 series microcontroller | Pass/Fail | Meets criterion | |
| **S2** | **1** | **CR7, CR1** | Communication/ Safety | **Report state of pack safety** | **ISO 11898-2 250kHz (high speed CAN)** | **Meets criterion** | |
| **S3** | **1** | **CR7, CR1** | | **Report state of charge of pack** | | | |
| **S4** | **1** | **CR7, CR1** | | **Report electrical metrics of pack** | | | |
| **S5** | **1** | **CR7, CR1** | | **Report faults within the pack** | | | |
| S6 | 2 | CR1, CR9 | Communication | Complete system data read time | ms | 100 | 25 |
| S7 | 1 | CR2 | Compliance | Size of internal HW | mm | ±2.5 | 60x175x25 |
| S8 | 1 | CR2 | | Size of external HW | mm | ±2.5 | 150x150x2 |
| **S9** | **1** | **CR5** | Performance | **Cell voltage measurement range** | **V** | **0-4.2** | **0-4.5** |
| S10 | 1 | CR5 | | Cell voltage measurement accuracy | mV | ±30 | ±5 |
| **S11** | **1** | **CR6** | | **Cell temperature measurement range** | **°C** | **0-100** | **0-150** |
| S12 | 1 | CR6 | | Cell temperature measurement accuracy | °C | ±2 | ±1 |
| S13 | 1 | CR3 | | Pack voltage measurement range | V | 0-400 | 0-400 |
| S14 | 1 | CR3 | | Pack voltage measurement accuracy | V | ±1 | ±0.1 |
| **S15** | **1** | **CR4** | | **Pack current measurement range** | **A** | **1-500** | **1-550** |
| S16 | 1 | CR4 | | Pack current measurement accuracy | A | ±5 | ±2 |
| S17 | 1 | CR4 | | State of charge (SOC) estimate accuracy | kWh | ±1 | ±0.1 |
| S18 | 3 | CR14 | | State of health (SOH) estimate accuracy | % | 20 | 5 |
| **S19** | **2** | **CR9, CR10** | Performance | **Time to full pack balance** | **h** | **3** | **< 2** |
| S20 | 1 | CR8 | Compliance | BMS powered by LVSS outputs | V | 5 | 5 |
| S21 | 3 | CR8 | | Maximum power consumption (from LVSS) | W | < 10 | < 5 |

In addition to the requirements set by our customer, the race that we intend to compete with REV2, Pikes Peak International Hill Climb, has its own safety requirements. Within the electric vehicle class, any high-voltage line coming from the main battery pack must be clearly marked as such, as well as properly insulated for the voltage. Additionally, any high voltage tap must be separately fused from the main motor-controller fusing.

## Description of Design

Our analysis of existing BMS architectures currently on the market led us to a few key approaches. When deciding between active and passive balancing, the dominant approach in the market is passive, due to its simplicity and cost effectiveness. The distribution of boards throughout a battery pack comes in two different configurations: centralized, and distributed. Several years ago, both of these were viable approaches to BMS design. In more recent years, with higher voltage EVs and more intelligent cell balancing ICs, a distributed architecture is more cost effective, while also capable of monitoring a much higher number of cells.

The team decided to go with a modular, master-slave architecture for the BMS. The main system is composed of 11 printed circuit boards (PCBs): one Master and ten Slaves. The Master is external to the REV2 pack,while the Slave is internal. This allows maximum efficiency and minimum size by keeping only the essential hardware in the pack interior.

The Master acts as the main controller of the BMS. The heart of the Master board is a 32-bit ARM Cortex M4 microprocessor by STMicroelectronics. It controls what the Slaves are doing, and

communicates metrics of packs to the rest of the bike in real time. The Master features a TI battery impedance tracking IC which calculates state of charge (SOC), which is analogous to a fuel gauge on a car. The board is powered by the 5V bus from the bikes low voltage subsystem.

The Slave boards are the direct interface with the batteries, and are internal to the battery pack. The only connection between the Master and the Slaves is a parallel 2-wire isolated SPI bus. The primary component on the Slave board is the LTC6811, by Linear Technology. The LTC6811 controls the balancing of the cells while also measuring cell voltage and temperature. The board is powered directly by the cells is connected to through the use of a 5V buck converter. Due to the need for flexibility of the cell count per Slave board, it was designed to accommodate between six and twelve cells.

Not only is the new design usable for the 400V battery pack of REV2, but it adds more features than BMS 3.3 while also being smaller and less expensive. The overall size and cost of our design is 60% of BMS 3.3[1]. BMS 4.0 utilizes a simpler architecture, easier to use and debug. It also features a dedicated state of charge IC, a new feature not implemented on previous versions.

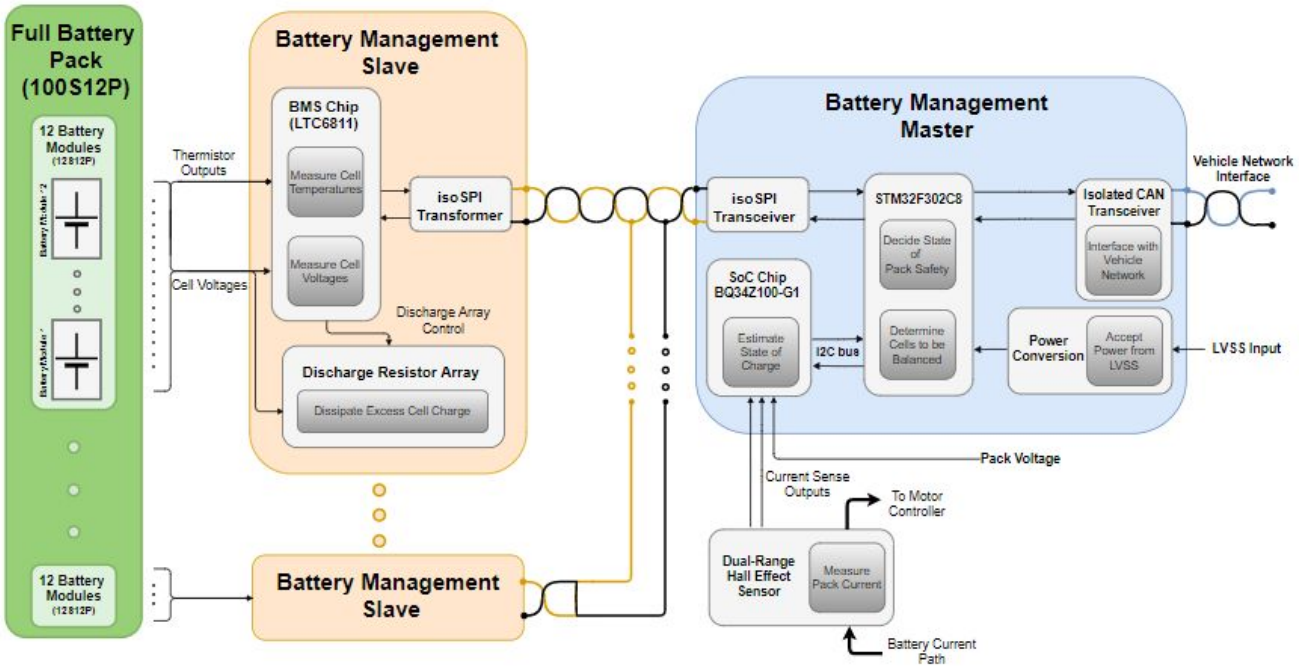


Figure XX: BMS 4.0 Functional Decomposition

The functional decomposition in Figure XX shows each board's responsibilities with respect to the engineering requirements. Another method used to keep track of requirements is traceability flowdown. For each major sub-system, such as the balance circuit and LTC6811 circuit, the requirements flowdown shows the relation between customer requirements, engineering requirements, and actual electrical functions. They also were designed to keep track of progress. Figure XX shows one example:

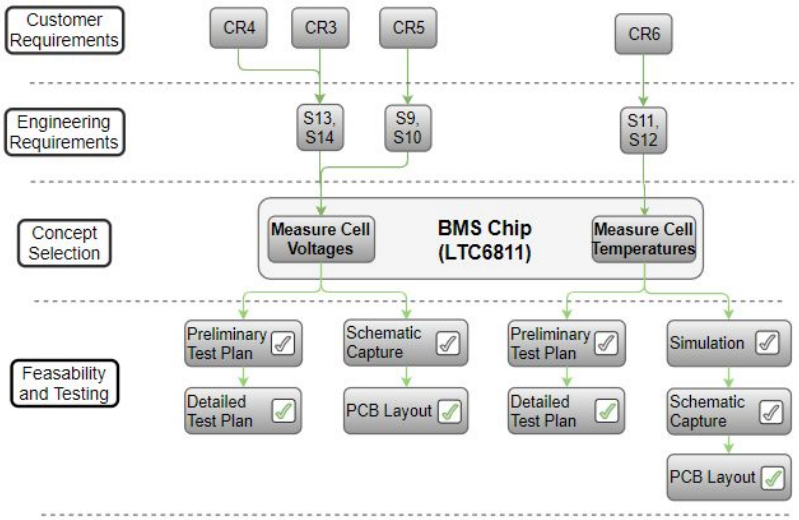


Figure XX: LTC6811 Requirement Flowdown Diagram

**Supporting Feasibility of Evidence**

Once we had our functions defined and traced back to the engineering requirements, the next step in the process was to decide how to physically implement them in hardware through the use of a morphological chart. Pugh analyses were done to determine the design with the optimal solutions. As a result of this process, the final design chosen is shown in Figure XX. This is the same design specified in the functional decomposition on Page XX.

| Design A | |
|---|---|
| Sub Function | Solution Chosen |
| Balancing Method | Passive |
| Thermal Management | PCB Thermal Relief |
| Temp Sensing | Thermistor |
| SoC Calculation | Dedicated Chip |
| Current Sensing | Multi-Range Hall Effect |
| BMS Chip | LTC6811 |
| Communications / Architecture | Multiple Solutions |
| Microcontroller Selection | STM32F302C8 |
| Emergency Pack Shutoff | Multiple Solutions |
| Safety | Multiple Solutions |

Figure XX: Design Chosen After Pugh Analysis of Morph Chart

*Simulation and Theoretical Mathematical Analysis*

One of our requirements was time for full pack balancing, which relates directly to how much cell balance current would be required. Calculations were performed to generate an optimal balance between cell balancing time and size of internal hardware due to increased power dissipation requirements.

$$I_{balance} = SOC\ error * Q_{cell} / t_{balance} \quad (1)$$

Building upon the feasibility analysis, SPICE models were developed to simulate the primary analog circuits. The circuits analyzed were the 5V regulator, the balancing array, and the temperature sense circuit on the Slave board. These simulations were used to verify basic functionality, study transient characteristics, and determine optimal values for passive components. Figure XX shows one example of the 5V supply circuit for the Slave board.

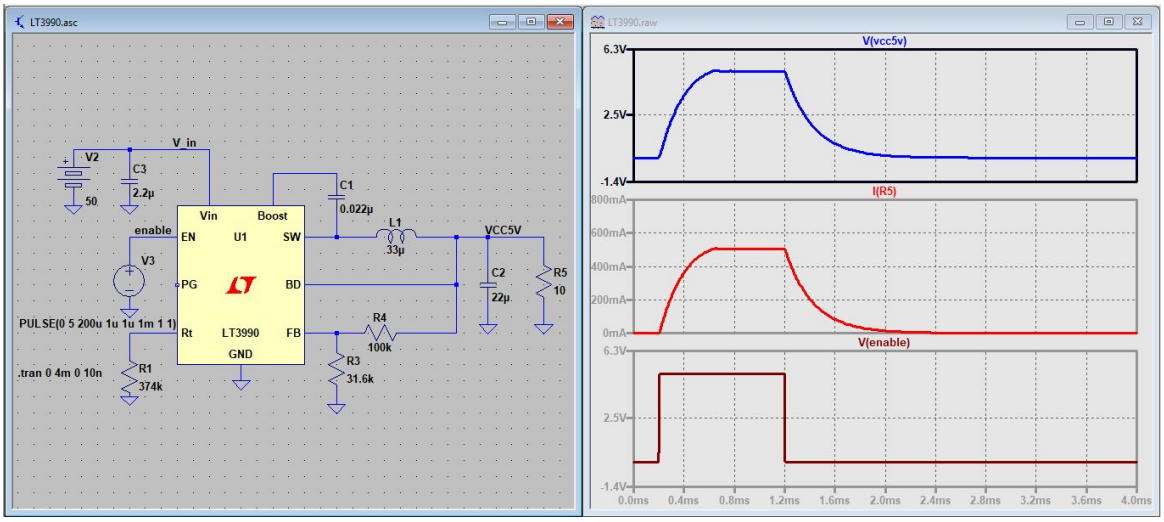


Figure XX: LT3990 Simulation (Slave Board 5V Supply Buck Converter)

*Concept Selection Through Feasibility Testing*

Some of the potential concepts were selected based off feasibility testing to compare similar solutions. For example, a quick comparison between current sensing methods was made early before making a decision. The figure below shows results of testing of a current shunt and dual-range hall effect current sensor on REV1. From the results, it was determined that the hall effect sensor was the best performing option.

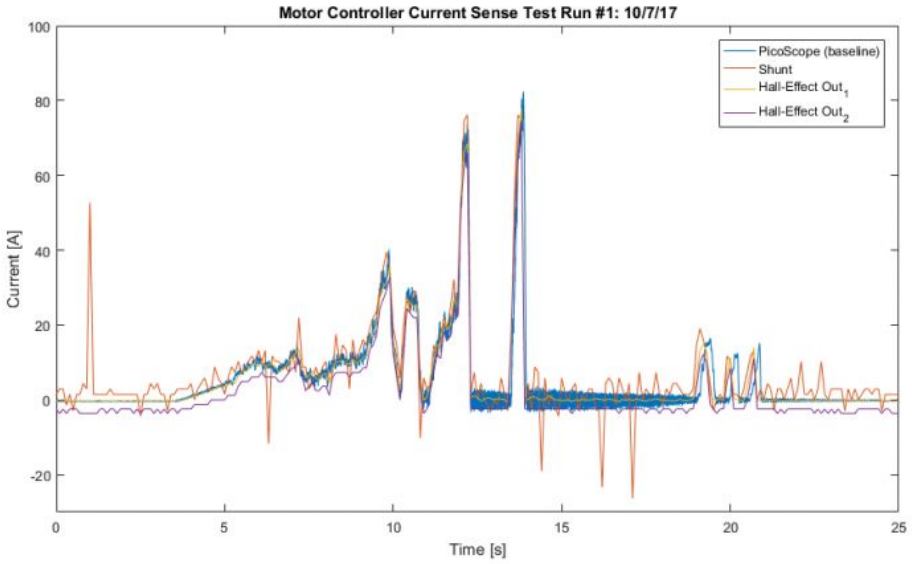


Figure XX: Battery Current Sensing Feasibility Test Results

*Demonstration of Design with Development Boards*

To properly evaluate each of the major components, evaluation kits were obtained and tested. The dev boards acquired were for the following components:

- STM32F302R8 Nucleo
    - A development board using an ARM Cortex M4 microprocessor in the same family as the chip used in our design. We used the STM Nucleo to verify some of the basic communication protocols, such as CAN and SPI.
- LTC Linduino
    - An Arduino-based microcontroller, tailored to using Linear Technology's development tools. The Linduino was used to test the LTC6811 demo board and the Slave board.
- LTC6811
    - The LTC6811 demo board allowed us demonstrate some of the functions of the IC before actually going through with the design.
- LTC6820
    - The LTC6820 converts normal 4-wire SPI to 2-wire isoSPI. The Master board utilizes the same circuit, so this board was used to test the functionality. It was also used in conjunction with the Linduino for preliminary Slave testing.
- TI BQ34Z100-G1
    - The Texas Instruments BQ34Z100-G1 impedance tracking state of charge (SoC) IC monitors the remaining charge in a battery pack over it's lifespan. In order to validate the

effectiveness of this IC with a larger battery pack, testing was slowly scaled from a single cell to the full pack voltage and current.

**Results**

The team's testing approach was to fully test each of the functions of both boards independently to find any design flaws, and then move towards full-system tests. Due to REV2's scheduled completion day well after the end of MSDII, the final test of the BMS would be on REV1, during an EVT test day. While the hardware configuration is not identical to what will be seen on REV2, it is similar enough to validate the performance of the designs in union with the rest of the tests we have done. This was determined to be the most accurate and effective evaluation of the project by the team, and was approved by our customer.

Master Test Results

The majority of the test plan for the Master boards was completed successfully. Features such as isoSPI and CAN communication interfaces were completely tested with the Slave board and some preexisting EVT hardware. Voltage and current measurement was validated to the extent of our testing equipment.

Two minor issues were discovered on Master 4.0: one of the SPI signals was missing a pull-up resistor, and the SOC chip was missing a thermistor input. These issues were resolved on the second revision of the board, Master 4.1.

Slave Test Results

Each of the primary functions of the Slave board were tested individually. Communications via isoSPI was confirmed using the Linduino and LTC6820 development board. The cell voltage and temperature readings were also confirmed. Accuracy of the LTC6811's ADCs were verified with a multimeter, shown in Table 3.

A few small issues were found with the 4.0 design during testing. The power resistors in the discharge array became very hot after a short balance cycle. The isoSPI termination resistor was put on the wrong side of the isolation transformer. It was discovered that the GPIO pins on the LTC6811 could not source current when configured as digital outputs. These design flaws were fixed in concurrent revisions.

Full System and Integration Test Results

Integration with REV1 was a success, mainly due to the careful communication between the various EVT sub-teams throughout the build process. By sharing 3D CAD models, accurate enclosures for the boards were made by EVT's mechanical team. Firmware was developed and tested alongside our hardware testing. The BMS voltage measurement functions were tested on REV1, with the results shown in Table XX. The team was pleased with the results, as most of the cell readings were exactly the same

as multimeter readings. The last cell in the stack was consistently off by a few millivolts, but were still within our margin of error based on the engineering requirements.

Table XX: Integration Test Results - Cell Voltage Measurements

| | Slave 0x4 | | | Slave 0x3 | | | Slave 0x0 | | | Slave 0x2 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Cell # | Actual | Slave | Diff | Actual | Slave | Diff | Actual | Slave | Diff | Actual | Slave | Diff |
| 1 | 3.623 | 3.623 | 0 | 3.642 | 3.643 | 0.001 | 3.856 | 3.856 | 0 | 3.845 | 3.845 | 0 |
| 2 | 3.633 | 3.633 | 0 | 3.64 | 3.641 | 0.001 | 3.859 | 3.858 | 0.001 | 3.804 | 3.803 | 0.001 |
| 3 | 3.637 | 3.638 | 0.001 | 3.643 | 3.644 | 0.001 | 3.866 | 3.867 | 0.001 | 3.848 | 3.848 | 0 |
| 4 | 3.639 | 3.639 | 0 | 3.642 | 3.643 | 0.001 | 3.859 | 3.857 | 0.002 | 3.861 | 3.861 | 0 |
| 5 | 3.648 | 3.648 | 0 | 3.645 | 3.646 | 0.001 | 3.869 | 3.869 | 0 | 3.86 | 3.861 | 0.001 |
| 6 | 3.524 | 3.524 | 0 | 3.645 | 3.645 | 0 | 3.834 | 3.834 | 0 | 3.861 | 3.861 | 0 |
| 7 | 3.594 | 3.594 | 0 | 3.639 | 3.626 | 0.013 | 3.804 | 3.804 | 0 | 3.857 | 3.842 | 0.015 |
| 8 | 3.646 | 3.631 | 0.015 | - | - | - | 3.87 | 3.73 | 0.14 | - | - | - |

The BMS was fully implemented on REV1 during a test day. The only major function not fully validated was the SOC function. All other functions were tested, and satisfy our engineering requirements.

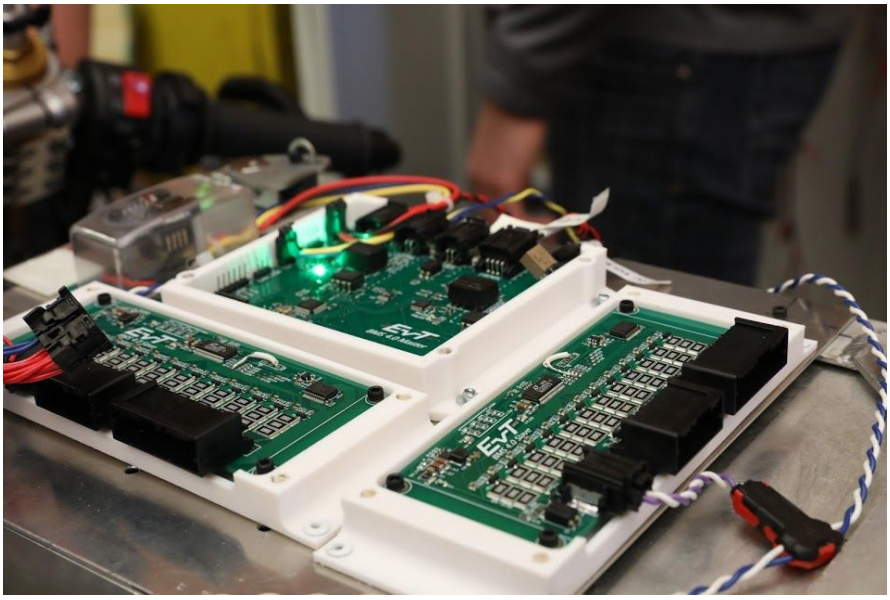

Figure XX: BMS 4.0 Installed on the REV1 Battery Pack

**Conclusions**

A total of 8 fully tested Slaves and 2 Masters were handed off to EVT. While firmware is still being refined at the time this paper was written, final deliverables of this project are complete. Great care has been taken to ensure that the research and work done by the team is available and easily understood for future generations of EVT members. Our customer, Alex Young, has expressed his

satisfaction with the current state of the system, and is eager to see it fully integrated with next generation electric motorcycle.

**Acknowledgements**

We would like to give a special thanks to our customer, Alexander Young, our Faculty Guide, Harold Pascal, and EVT's Faculty Advisor, Carlos Barrios.

Thank you to our sponsors:
Linear Technology
Altium
Texas Instruments